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Channel Temperature Measurement of GaN HEMT Used in Kilowatt-Level Power Amplifier

Sheng Zhong [1,2], Wenrao Fang [2,*], Juan Zhao [2], Wenhua Huang [2], Chao Fu [2], Lulu Wang [2] and Tianwei He [1,2]

[1] Department of Engineering Physics, Tsinghua University, Beijing 100084, China; zhong-s19@mails.tsinghua.edu.cn (S.Z.)
[2] Science and Technology on High Power Microwave Laboratory, Northwest Institute of Nuclear Technology, Xi'an 710024, China
* Correspondence: fangwenrao13@tsinghua.org.cn; Tel.: +86-029-84767845

Abstract

This paper presents an electrical thermometry method designed for kilowatt(kW)-level Gallium Nitride (GaN) High Electron Mobility Transistors (HEMTs). The dependence of the drain current on the channel temperature in GaN HEMTs is utilized as a means to measure the transient channel temperature. However, in kW-class GaN HEMTs, the gate current can reach tens of milliamperes, and trap-induced capture resulting from high doping concentrations can both influence the drain current. Through modifications to the gate bias circuit, the gate voltage self-biasing phenomenon caused by the gate current is mitigated. A theoretical model is derived to express the relationship between the drain current and the channel temperature. Experimentally, amplifier modules equipped with kW-level HEMTs were placed on thermal stages set at 45 °C, 60 °C, and 80 °C. The transient drain current curves and the corresponding channel temperature profiles were measured. The measured drain current versus channel temperature curves at different ambient temperatures were fitted and compared with the theoretically derived formula. The relative error between the measured and calculated drain current values at the same channel temperature was found to be within 1%.

Keywords: Kilowatt-level power amplifier; GaN HEMT; channel temperature; drain current

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1. Introduction

Gallium Nitride (GaN) semiconductors offer advantages such as high electron saturation velocity and high breakdown electric field strength, making them widely used in high-power microwave power amplifiers [1,2]. In recent years, with applications in deep-space exploration and phased array radar systems, GaN HEMTs have been progressively miniaturized and integrated, while their output power has been increased to the kilowatt (kW) level [3]. For kW-level GaN HEMTs, high power density leads to significant heat generation. Sustained heat accumulation causes a rapid rise in temperature, resulting in performance degradation. Excessive temperature may even cause thermal breakdown and failure [4]. Therefore, temperature is a key factor limiting further increases in the power capacity of GaN HEMTs. To prevent excessively high operating temperatures due to continuous heat accumulation, these power amplifiers are often operated under narrow-pulse-width and low-duty-cycle conditions. Consequently, for kW-level GaN HEMTs, temperature measurement under narrow pulses and low duty cycles is crucial for the reliability of design and engineering applications of high-power microwave power amplifiers [5].

There are three main approaches to temperature measurement of GaN HEMTs:

(1) Optical temperature measurement techniques: such as infrared thermography, Raman spectroscopy, and thermoreflectance imaging, can directly acquire die-temperature data [6]. However, optical thermometers with microsecond-level temporal resolution and micrometer-level spatial resolution are extremely expensive and often require dedicated device samples and specialized equipment [7], which are generally inaccessible in many electronics laboratories.

(2) Three-dimensional modeling and simulation: constructing a three-dimensional finite element model based on the HEMT's structure and material parameters to simulate the temperature distribution [8,9]. The advantage of this approach is the rapid acquisition of temperature profiles with extremely high spatial resolution. Nevertheless, accurate simulation requires precise structural dimensions of the transistor, which are often not fully disclosed by manufacturers due to confidentiality issues. Moreover, most mainstream thermal simulation software relies on Fourier's law, which has certain limitations at micrometer-scale dimensions, making it difficult to accurately predict heat transfer processes [10].

(3) Electrical measurements: indirect identification procedures from electrical measurements [11,12], which indirectly measure the temperature based on the dependence of electrical parameters on temperature. It is usually measured through electrical parameters with higher temperature sensitivity, such as threshold voltage and drain current [13,14]. The advantage of the electrical measurement method is that it can be rapidly measured using standard equipment and does not require direct contact with the power amplifier. Nevertheless, there are multiple factors influencing kW-class GaN HEMTs, such as the relatively large gate leakage current affecting the gate voltage and the trap effect influencing the drain current [15,16]. As a result, temperature is no longer a single variable of the drain current, making it difficult to accurately reflect the temperature variation by measuring the drain current.

For the first time, this study presents an electrical measurement method designed for kW-level GaN HEMTs. Modifying the series resistor and parallel capacitor in the gate bias circuit minimizes the gate leakage current's influence on the gate voltage, thereby reducing its impact on the drain current. The drain current waveforms were measured using a current clamp under ambient temperatures of 45 °C, 60 °C, and 80 °C, while the corresponding channel temperature was monitored by infrared thermography. A temperature-dependent current variation formula was derived based on experimental data at 45 °C. This formula was then used to establish a fitting model describing the relationship between current and temperature. The trap capture constant of the kW-level GaN HEMT was determined by comparing the formula-derived curves with experimental results. Furthermore, the validity of the fitting model was confirmed under conditions without trap effects, demonstrating its ability to accurately characterize current variations with channel temperature across different ambient temperatures. Consequently, real-time temperature estimation can be achieved by monitoring transient drain currents.

2. Detailed Analysis of the Proposed Method

2.1. Derivation of Drain Current Equations

In a high-power GaN HEMT, the directional movement of two-dimensional electron gas in the channel forms the drain current, and the electron concentration n_s can be expressed as [17]:

$$n_s(X,Y) = \frac{\varepsilon(x)}{q(d+D)}[V_G - V_T - V(Y)] \quad (1)$$

where $\varepsilon(x)$ is the dielectric constant of the AlGaN layer, q is the elementary charge, d is the thickness of the AlGaN barrier layer, D is the channel thickness, V_G is the gate voltage, $V(Y)$ is the potential distribution along the channel length, and V_T is the threshold voltage. By integrating the electron concentration along the channel length (Y-direction), the drain current I_{ds} is derived as [18]:

$$\begin{aligned} I_{ds} &= \int_0^L q n_s(X,Y) W v(\mathrm{E}) dY \\ &= \int_0^L q n_s(X,Y) W \mu E dY \\ &= \int_0^L q n_s(X,Y) W \mu dV \\ &= \int_0^L \frac{W\mu\varepsilon(x)}{(d+D)} [V_G - V_T - V(Y)] dV \\ &= \frac{W\mu\varepsilon(x)}{2L(d+D)} \left[2(V_G - V_T)V_{ds} - V_{ds}^2\right] \end{aligned} \tag{2}$$

where W is the gate width, L is the channel length, μ is the electron mobility, and V_{ds} is the drain voltage. When $\mathrm{d}I_{ds}/dV_{ds} = 0$, the solution yield is $V_{ds} = V_G - V_T$. The physical quantities that change with temperature in the drain current expression formula include electron mobility $\mu(T)$ and threshold voltage $V_T(T)$ [19]. When the power amplifier works in the saturation region, $V_{ds} \geq V_G - V_T$, the drain current $I_{ds}(T)$ formula can be expressed as:

$$I_{ds}(T) = \frac{W\mu(T)\varepsilon(x)}{2L(d+D)} (V_G - V_T(T))^2 \tag{3}$$

where $I_{ds}(T)$, $\mu(T)$ and $V_T(T)$ is the drain current, carrier mobility, and threshold voltage at the channel temperature T. Electron mobility $\mu(T)$ decreases with increasing temperature, and its change with temperature can be described as [20]:

$$\mu(T) = \mu(T_0) \left(\frac{T}{T_0}\right)^{-k_1} \tag{4}$$

where T is the channel temperature, T_0 is the ambient temperature, $\mu(T_0)$ is the electron mobility at the ambient temperature T_0 and k_1 is a constant. The threshold voltage of the HEMT decreases almost linearly with increasing temperature and can be described as [20]:

$$V_T(T) = V_T(T_0) - k_2(T - T_0) \tag{5}$$

where $V_T(T_0)$ is the threshold voltage at a channel temperature of T_0 and k_2 is a constant. Therefore, as the temperature increases, the drain current will decrease as the carrier mobility decreases, and increase as the threshold voltage decreases. When the drain current is large, the carrier mobility change caused by temperature change has a greater effect on the drain current. When the drain current is small, the influence of threshold voltage is greater.

For a GaN HEMT with output power up to kilowatts, the drain current generally ranges from tens of amps to hundreds of amps. The main reason for the drain current change is carrier mobility, and the threshold voltage change is relatively negligible. Consequently, the relationship between drain current $I_{ds}(T)$ and temperature can be expressed as [21]:

$$I_{ds}(T) = I_{ds}(T_0) \left(\frac{T}{T_0}\right)^{-k} \tag{6}$$

where $I_{ds}(T_0)$ is the drain current at a channel temperature of T_0.

2.2. Key Factors Influencing Drain Current

For a GaN HEMT, when an external pulsed voltage signal is applied, I_{ds} represents the response to the V_{ds} excitation, exhibiting a trend depicted in Figure 1a. As derived

from Formulas (2) and (3), I_{ds} is primarily dependent on the V_{gs}, trap effects, and temperature [22,23].

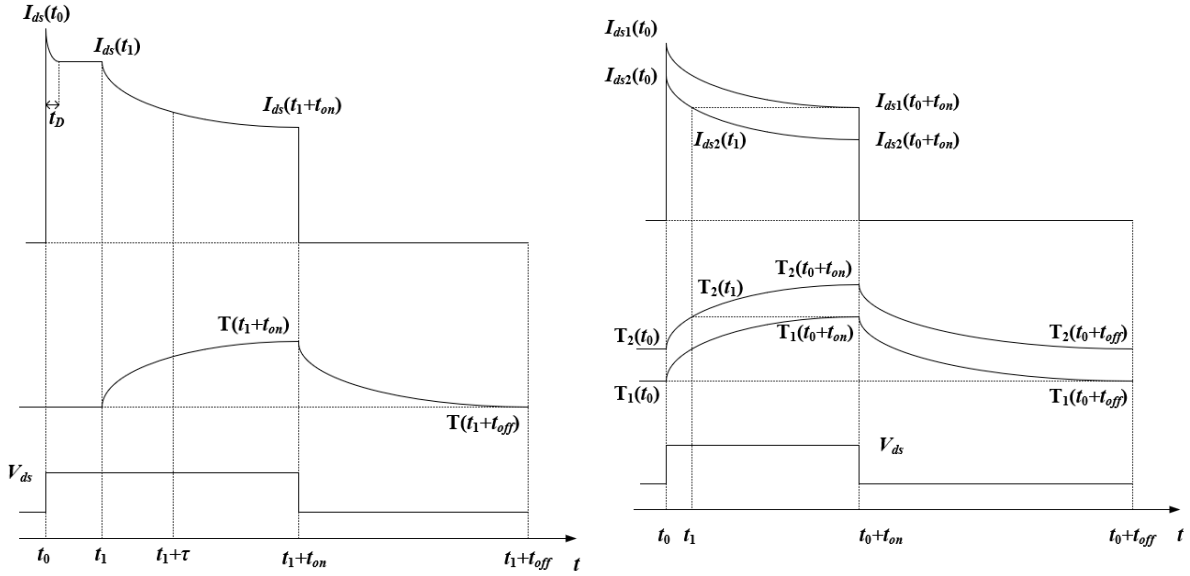


Figure 1. (**a**) Drain current and channel temperature waveforms corresponding to a drain voltage pulse. (**b**) Time-domain waveforms of the drain current and channel temperature corresponding to the same drain voltage pulse and different ambient temperatures.

2.2.1. Gate Voltage

Experiments have revealed that GaN HEMTs exhibit a significant number of defects, with a surface state trap density at the AlGaN/GaN interface of approximately 10^{13} cm^{-2} [24]. The gate leakage current and carrier concentration are correlated with the surface state trap density [25]. As a result, kW-level GaN HEMTs exhibit substantial gate leakage current. This gate current induces a voltage drop across the gate bias circuit, thereby affecting the gate voltage. Reducing the resistance of the gate bias circuit can mitigate variations in the gate voltage. To counteract the negative resistance effect, GaN HEMTs require a stabilized gate bias circuit, typically implemented using an RC parallel structure [26]. This study modifies the conventional RC parallel circuit composed of a 4.7 Ω resistor and a 10 μF capacitor by reducing the gate resistor to 0.5 Ω and increasing the number of parallel capacitors. The circuit schematic is shown in Figure 2. At high frequencies, capacitors exhibit parasitic resistance and inductance. Figure 3 shows the simulated frequency-dependent S-parameters obtained using ADS 2022 software. The optimized design demonstrates improved filtering performance in the gate bias circuit. The resistance and capacitance values of the modified bias circuit were selected based on the oscillation frequency observed without the bias circuit, and this method is scalable to different power levels.

2.2.2. Trap Effect

When V_{gs} remains constant within the drain voltage pulse, I_{ds} is predominantly influenced by trap effects and temperature. It is generally acknowledged that trap capture occurs within a very short duration (approximately 50 ns) after the application of the drain pulse voltage [27], but this process is sufficiently rapid to elude detection by even the most advanced narrow-pulse measurement systems. However, Ref. [28] revealed the existence of trap capture with millisecond-level time constants (τ) in a GaN HEMT. The temperature impact on I_{ds} encompasses both ambient temperature and self-heating-induced temperature

rise. For pulsed-power amplifiers, self-heating causes the junction temperature to increase gradually during the pulse, consequently leading to a monotonic decrease in I_{ds} over time.

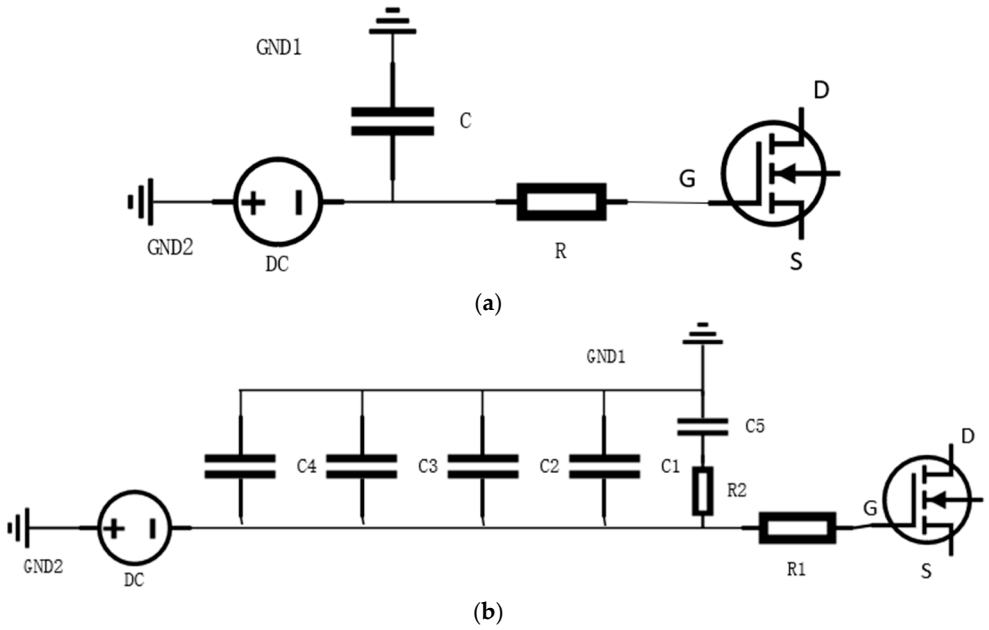


Figure 2. (**a**) Traditional gate bias circuit. (**b**) The proposed gate bias circuit.

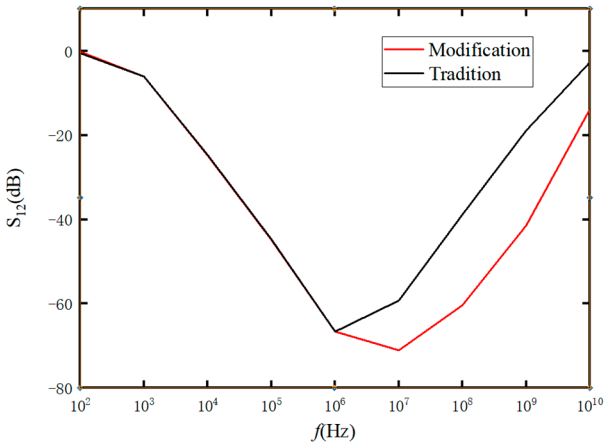


Figure 3. Measured S-parameters of the traditional gate bias circuit and the proposed gate bias circuit.

Therefore, during the interval from the pulse onset (t_0) to the trap capture time constant (τ), the variation in I_{ds} is governed by both trap capture dynamics and thermal effects. Beyond τ until the pulse termination (t_{off}), the decline in I_{ds} is attributed almost exclusively to the temperature rise induced by self-heating. If the assumption holds that I_{ds} magnitude is solely temperature-dependent, then under different ambient temperatures, identical I_{ds} values should be measured when the junction temperature is the same and the pulse width exceeds the trap capture time constant τ. Figure 1b illustrates schematic waveforms of drain current and chip temperature under the same drain voltage pulse but different ambient temperatures $T_1(t_0)$ and $T_2(t_0)$. When $T_2(t_1) = T_1(t_0 + t_{on})$, the measured drain current $I_{d2}(t_1) = I_{d1}(t_0 + t_{on})$. Since the *k*-value is independent of ambient temperature, the *k*-value derived from drain current and chip temperature measurements under room temperature can be used to fit the chip temperature curve from drain current data acquired under varying ambient temperatures. This approach ultimately enables the measurement of chip temperatures under extreme environmental conditions.

3. Measurement Setup of the Proposed Method

Based on the above analysis, the k-value in Formula (6) can be determined by measuring the drain current under a short pulse width and the temperature at the power amplifier chip, thereby deriving the current-temperature variation curve through fitting.

For kW-level pulsed GaN HEMTs, the typical operating pulse width is 5 μs with currents ranging from tens to hundreds of amperes. This measurement used an X-band GaN HEMT to validate the relationship between drain current and temperature [29]. To minimize the drain bias circuit path, a dedicated slot was designed in the test fixture to accommodate the current clamp for drain current measurement. The DC circuit can convert an input continuous voltage signal into a square wave signal, with both the rise time and fall time under 50 ns. Figure 4 illustrates the schematic diagram and physical setup of the drain current waveform measurement.

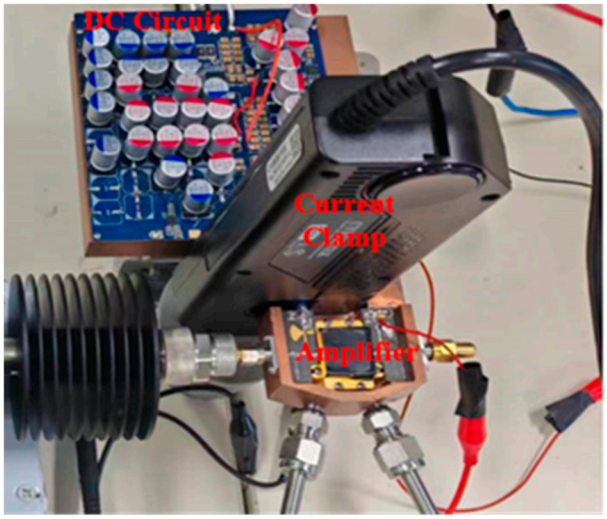


Figure 4. Drain current waveform measurement system.

An infrared microscope was used to measure the channel temperature of the power amplifier, and the measurement diagram and infrared detection interface are shown in Figure 5. The infrared detector has a time resolution of the order of μs, so it can only measure the channel temperature change after the initial temperature and the working pulse width of 1 μs [30].

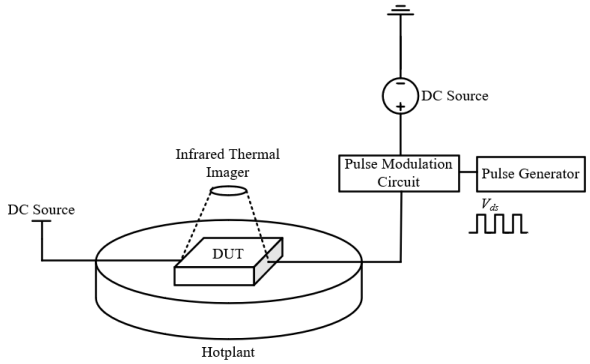


Figure 5. Schematic diagram of infrared temperature measurement.

4. Results and Discussion

With Vgs set to −1 V and Vds to 60 V, the drain voltage pulse width was configured to 3 μs and the cycle period to 3 ms. The gate voltage and drain current waveforms of the power amplifier were measured at an ambient temperature of 25 °C. The measurement

results for both the conventional bias circuit and the optimized practical bias circuit are shown in Figure 6.

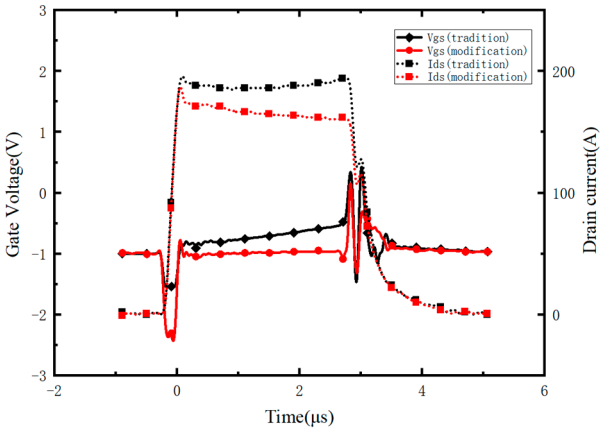


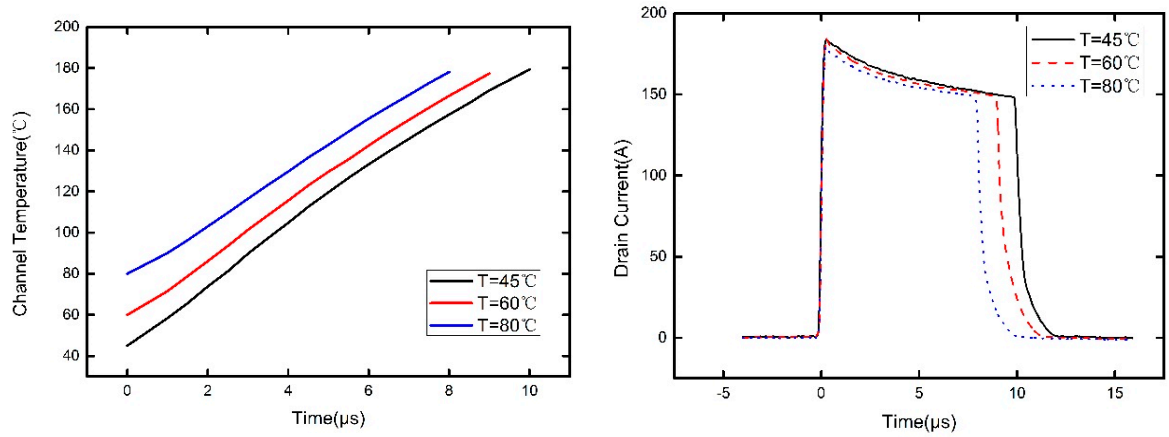
Figure 6. Drain current and gate voltage waveforms under traditional measurement condition and modified grid circuit condition.

The drain current with the conventional bias circuit did not decrease gradually as theoretically expected due to the rising junction temperature during operation. Instead, after an initial decrease, it gradually increased. This behavior is attributed to the gate current slowly rising over time, leading to a corresponding gradual increase in the voltage drop across the bias circuit. Over the 3 μs pulse duration, the gate voltage increased by approximately 0.5 V. The rise in gate voltage resulted in an increase in carrier concentration within the channel, thereby elevating the drain current. Although temperature rise typically causes a reduction in drain current, according to Equation (6), the influence of temperature on drain current diminishes at higher temperatures.

Therefore, during the first half of the pulse width, the decrease in drain current—driven by junction temperature rise and trap effects—dominates the current variation. In the latter half, as trap effects weaken and the temperature's influence on current variation decreases, the increase in drain current caused by the rising gate voltage becomes the dominant factor. This leads to the observed trend where the current first decreases and then increases.

To ensure that the drain current is solely influenced by temperature variation, it is essential to maintain a constant gate voltage. This study proposes a modified bias circuit that reduces the series gate resistance Rg and adjusts the parallel gate-to-ground capacitance. Under the conditions of Vgs = −1 V, Vds = 60 V, and a drain voltage pulse width of 3 μs, the measured gate voltage is shown in Figure 6. The maximum value recorded during the 3 μs operational pulse was −0.97 V, representing a 94% reduction in gate voltage variation compared to the conventional bias circuit. This modification effectively eliminates the influence of gate voltage fluctuation on the drain current.

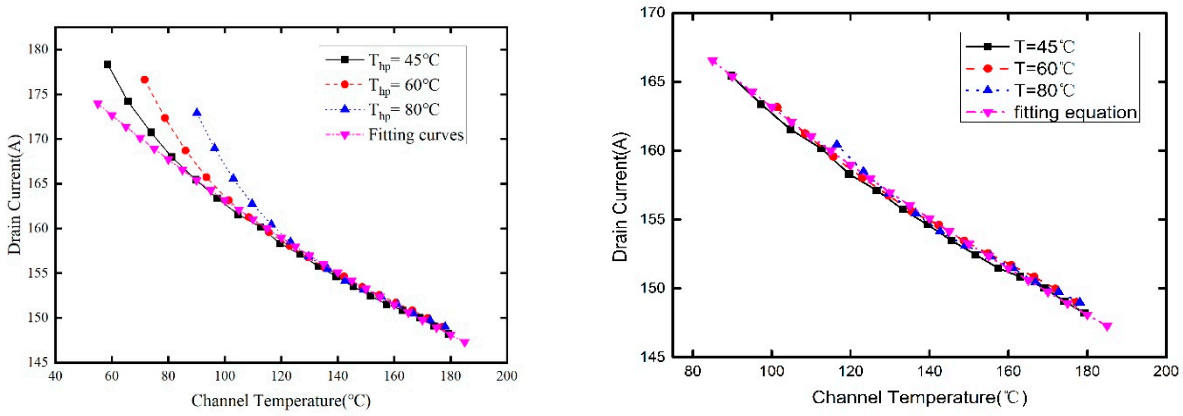
After adjusting the gate bias circuit, we established a measurement system for drain current and channel temperature. Under hotplate temperatures (T_{hp}) of 45 °C, 60 °C, and 80 °C, the drain current curve of the power amplifier was measured using a current clamp, while the temperature profiles of the channel were captured via an infrared thermal imager. The measured curves are shown in Figure 7. The pulse widths used at hotplate temperatures of 45 °C, 60 °C, and 80 °C were 8 μs, 9 μs, and 10 μs, respectively. At these pulse widths, the max channel temperature of the power amplifier is 180 °C, as shown in Figure 7a.



(**a**) (**b**)

Figure 7. Comparison of the channel temperature waveform (**a**) and the drain current waveform (**b**) under different hotplate temperatures.

Under a 45 °C hotplate environment, the measured drain current and corresponding channel temperature values were substituted to calculate k = 0.5 in Formula (6). Figure 8a presents the drain current versus channel temperature curves fitted using data measured at the same time point under hotplate temperatures of 45 °C, 60 °C, and 80 °C, along with the fitting curve from Equation (6). Figure 8b shows the drain current versus temperature curves fitted using drain current and channel temperature data taken at the same time point within the 3 μs to 10 μs interval under the same hotplate temperatures, also accompanied by the fitting curve from Equation (6). A comparison between Figure 8a,b indicates a trap time constant of 3 μs, and the extracted 3 microsecond trap time constant is generalizable across measured devices. Within the time range of 3 μs to 10 μs, the relationship between drain current and temperature aligns with the characterization by Equation (6) in Section 2.1, thereby validating the analysis in Section 2.2.2 and Figure 3.



(**a**) (**b**)

Figure 8. Temperature-dependent variation curves of all time (**a**) and post-3 μs (**b**) drain current and formula-fitted current values under different hotplate temperatures.

The k-value is independent of ambient temperature. As shown in Figure 8, the drain current remains consistent at a given channel temperature, regardless of the hotplate temperature. However, the k-value is dependent on the drain bias voltage. Therefore, recalibration would be required if a different drain bias voltage is applied or if devices from a different process node are used, in order to accurately determine the k-value.

It is evident that during the initial period after the drain pulse voltage V_{ds} is applied to the HEMT, the internal current is simultaneously influenced by both self-heating effects and trapping effects. For the tested kW-level GaN HEMT, the fitting formula curve represents the magnitude of the current decline due to temperature. In the 0~3 μs timeframe, the trapping effect further accelerates the drain current drop [15]. Beyond this period, the drain current continues to decrease, but the decline is almost exclusively attributed to the self-heating-induced temperature rise in the HEMT. Based on this analysis, the measured current and channel temperature data from the post-3 μs timeframe under different ambient temperatures were selected for fitting, as illustrated in Figure 8. Figure 8 demonstrates that under identical gate and drain voltages, the drain current magnitude is predominantly governed by the channel temperature, as thermal effects alone dominate the current behavior at this stage [20,28,31]. The individual contributions of self-heating and trap trapping are illustrated in Figure 8a. Taking the test results of the 45 °C environmental hot stage as an example, the fitted curve indicates that self-heating accounts for a current reduction of 7 A, meaning that trap trapping is responsible for the remaining 5 A decrease.

By neglecting the impact of trapping effects, the measured current values beyond 3 μs were compared with formula-fitted results. Their absolute and relative errors are shown in Figure 9, which demonstrates an absolute error below 1 A and a relative error less than 0.6%. The experimental results confirm that when the operational pulse width is sufficiently long, the measured drain current under different ambient temperatures is jointly influenced by both trapping effects and self-heating effects within the first 3 μs of the working pulse. Beyond 3 μs, the drain current decline is almost exclusively governed by self-heating effects, with the current magnitude solely dependent on the channel temperature.

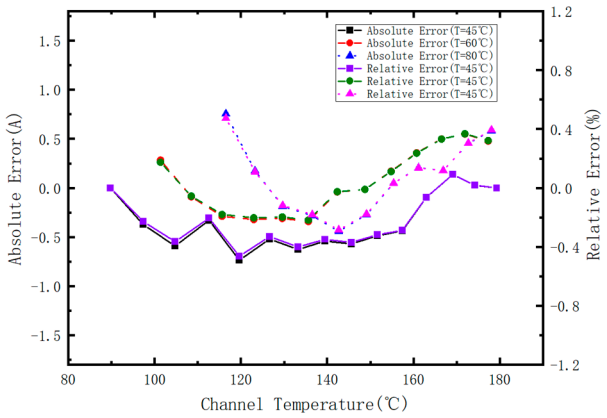


Figure 9. Absolute error and relative error between the measured post-3 μs drain current and the formula-fitted results.

5. Conclusions

This paper proposes an electrical thermometry method for measuring the channel temperature of a kW-level GaN HEMT. For high-power GaN HEMTs operating in pulsed mode, the channel temperature directly affects output characteristics such as carrier mobility, drain current, and output power. Furthermore, a higher temperature significantly increases the risk of thermal breakdown and permanent damage to the HEMT. Therefore, monitoring the instantaneous temperature within the pulse is critically important. By modifying the series resistance and parallel-to-ground capacitance in the gate bias circuit, the influence of gate leakage current on gate voltage is minimized to stabilize the gate bias. Based on the derived formula correlating drain current with channel temperature, a comparison with experimental measurements not only yields a trapping time constant of 3 μs but also demonstrates that, under different ambient temperatures, when the duration within the drain voltage

pulse exceeds this trapping time constant, the drain current depends solely on channel temperature. By adopting this method, the channel temperature of GaN HEMTs from the same manufacturing process can be tested quickly and accurately after calibration. This effectively solves the problem faced by electrical laboratories that lack microsecond-level optical thermometers, enabling them to measure the transient temperature within pulses.

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