Scientific Research Publishing

Circuits and Systems, 2024, 15, 13-27
https://www.scirp.org/journal/cs
ISSN Online: 2153-1293
ISSN Print: 2153-1285

Performance Study of a Quadratic Boost Converter

Modou Badiane[1], Prince Abdoul Aziz Honadia[2], Oumar Diallo Sadio[1], Fabé Idrissa Barro[1*]

[1]Department of Physics, Semiconductors and Solar Energy Laboratory, Faculty of Science and Technique, Cheikh Anta Diop University, Dakar, Senegal
[2]Renewable Thermal Energy Laboratory, Kaya University Centre, Ouagadougou, Burkina Faso
Email: modoubadiane99@gmail.com, prince1346@yahoo.fr, oumar.sadio@yahoo.fr, *fabe.barro@ucad.edu.sn

How to cite this paper: Badiane, M., Honadia, P.A.A., Sadio, O.D. and Barro, F.I. (2024) Performance Study of a Quadratic Boost Converter. *Circuits and Systems*, **15**, 13-27.
https://doi.org/10.4236/cs.2024.152002

Received: November 14, 2023
Accepted: February 26, 2024
Published: February 29, 2024

Abstract

Energy is the driving force behind all economic and industrial development. Africa is the least advanced continent in terms of energy consumption and production. Paradoxically, it is the sunniest continent, which is why our objective is to exploit this energy potential in order to produce and use sufficient energy. To achieve this, we are carrying out a series of studies aimed at developing a device capable of converting solar photovoltaic energy into electrical energy. This device is a two-stage converter, the first of which is a quadratic boost and the second a full bridge. Initially, this paper is devoted to studying the performance of the quadratic boost.

Keywords

Solar Energy, Photovoltaic, Efficiency, Quadratic Boost Converter

1. Introduction

Power DC/DC converters have plenty of topologies, and the corresponding conversion technique is a big research topic. By an uncompleted statistic, there are more than 500 topologies of power DC/DC converters existing [1].

Three types of fundamental DC/DC topologies were constructed, which are **Buck** converter, **Boost** converter and **Buck-Boost** converter. They can be derived from single-quadrant operation choppers. For example, buck converter was derived from A-type chopper. These converters have two main problems: linkage between input and output, and very large output voltage ripple. Boost converter is a step-up DC/DC converter. It works in the second-quadrant operation. It can be derived from Quadrant II chopper. And the Buck-boost converter is a step-down/up DC/DC converter. It works in the third quadrant operation.

This paper proposes quadratic boost converter (QBC) topology.

This article is part of a series of works whose aim is to convert a DC voltage from a photovoltaic system to an AC voltage. This conversion must be carried out using a two-stage converter, the first of which is a quadratic boost converter and the second a full bridge. Firstly, we will study the performance of the first stage using a solar module with a nominal voltage of 17.

2. Modeling the Quadratic Boost Converter

There are several types of quadratic boost converters, each with a well-defined switching mode. These configurations include: the Rotated Cell Single Switch (RC***S2-QB***), the Software Synthesized Single Switch (***S4-QB***), the Cascaded Connected Double Switch (***C2DS-QB***) and the Cascaded Connected Single Switch (***C2S2-QB***) [2]. These different types of configurations are shown in Figure 1.

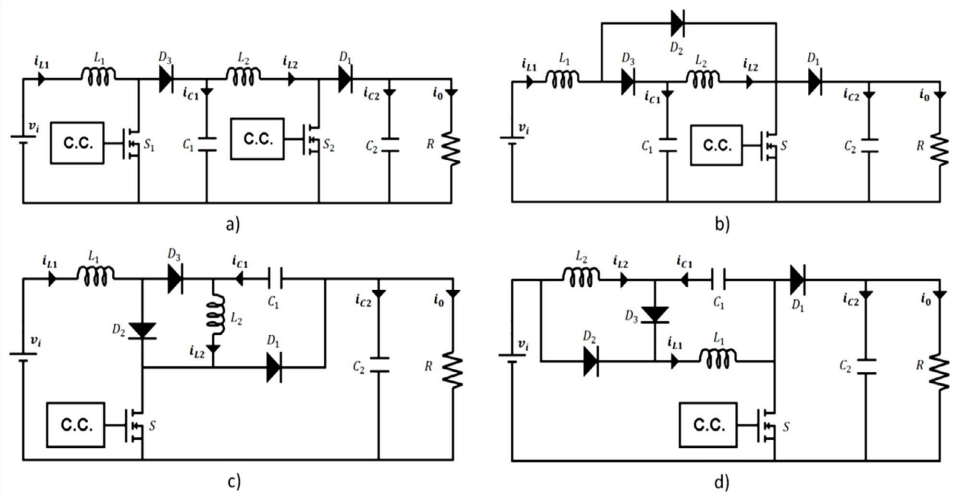


Figure 1. Diagram of quadratic boost converter topologies: a) C^2DS-QB; b) C^2S^2-QB; c) RCS^2-QB; d) S^4-QB.

For this study, we chose the quadratic boost with a single transistor switch, *i.e.* the C^2S^2-QB.

These different modes of switching on and off are shown in Figure 2.

Figure 2 shows that if the system structure changes from off to on at the start of the switching period, and from on to off when the interval defined by the duty cycle of the control signal has elapsed, then the converter operates in CCM. On the other hand, in the DCL1 and DCL2 conduction modes illustrated, the converter switches from the off state to the DCL1 or DCL2 state, then back to the on state at the start of a new switching period Figure 3.

Furthermore, the converter can operate either in DCL12 mode, arriving in DCL12 state from DCL1 state, or in DCL2 mode from DCL1 state, or in DCL21 mode arriving in DCL12 state from DCL2 state.

The difference between these two modes lies in which state is reached first after the stop state [3].

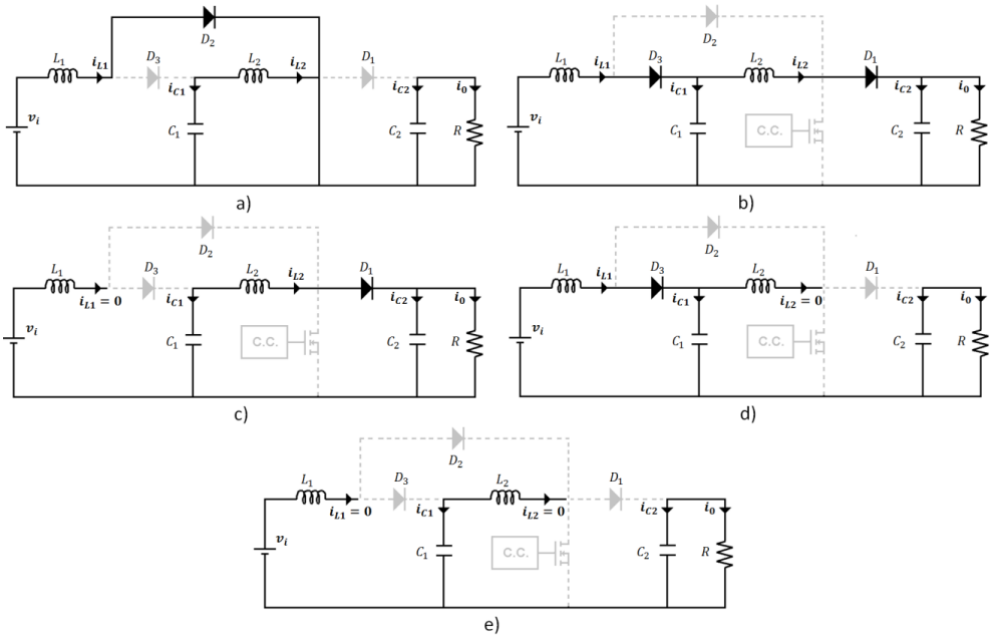


Figure 2. Quadratic boost converter state circuit diagrams: (a) active state; (b) inactive state; (c) DCL1 state; (d) DCL2 state; and (e) DCL12 state.

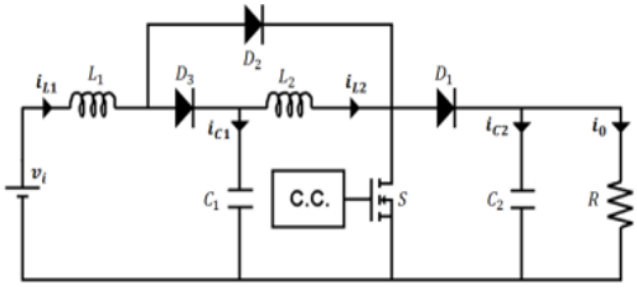


Figure 3. Basic diagram of quadratic boost converter.

3. Equations and Dimensioning

The two sets of equations above represent the equations of state of the quadratic boost converter in the on-state and off-state, respectively. It is always preferable to take an average model for such switching converters. The average model is given in Equation (3). The transfer function can be easily derived from this state-space average model

$$\begin{bmatrix} \dot{\hat{i}}l_1 \\ \dot{\hat{i}}l_2 \\ \dot{\hat{v}}c_1 \\ \dot{\hat{v}}c_2 \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1-D}{L_1} & 0 \\ 0 & 0 & \frac{1}{L_2} & -\frac{1-D}{L_2} \\ -\frac{1-D}{L_1} & -\frac{1-D}{L_1} & 0 & 0 \\ 0 & \frac{1-D}{C_2} & 0 & -\frac{1-D}{RC_2} \end{bmatrix} \begin{bmatrix} \hat{i}L_1 \\ \hat{i}L_2 \\ \hat{v}c_1 \\ \hat{v}c_2 \end{bmatrix} + \begin{bmatrix} \frac{E}{(1-D)L_1} & \frac{1}{L_1} \\ \frac{E}{(1-D)^2 L_2} & 0 \\ -\frac{E}{(1-D)^4 RC_1} & 0 \\ -\frac{E}{(1-D)^3 RC_2} & 0 \end{bmatrix} \begin{bmatrix} \hat{d} \\ \hat{e} \end{bmatrix}$$

So we can define a transfer function that represents the ratio between the output voltage and the duty cycle

$$G(S)=\frac{\hat{V}_{0ut}(S)}{\hat{d}(s)}=\frac{g_3S^3+g_2S^2+g_1S+g_0}{S^4+a_3S^3+a_2S^2+a_1S+a_0}$$

where the coefficients are given in the following lines

$$g_3=\frac{V_i}{(1-D)^3C_2R}$$

$$g_2=\frac{-V_i}{(1-D)L_2C_2}$$

$$g_1=V_i\left[\frac{2L_1}{(1-D)^3C_1C_2L_1L_2R}\right]$$

$$g_0=\frac{-2V_i(1-D)}{L_1L_2C_1C_2}$$

$$a_3=\frac{1}{C_2R}$$

$$a_2=\frac{1}{L_2C_1}+\frac{(1-D)^2}{L_2C_2}+\frac{(1-D)^2}{L_1C_1}$$

$$a_1=\frac{1}{L_2C_1C_2R}+\frac{(1-D)^2}{L_1C_2C_1R}$$

$$a_0=\frac{(1-D)^4}{L_1C_2C_1R}$$

For PID control, we will present a calculation method for determining the corrector coefficients.

The first step is to choose an overrun coefficient M_p of between 15% and 20%. This will enable us to determine the following Relationship:

$$\zeta=\sqrt{\frac{\ln^2(M_p)}{\ln^2(M_p)+\pi^2}}$$

$$PM=\arctan\left(\frac{2\zeta}{\sqrt{-2\zeta^2+\sqrt{4\zeta^4+1}}}\right)$$

$$G(s)=\frac{(s+z_1)(s+z_2)(s+z_3)}{(s+p_1)(s+p_2)(s+p_3)(s+p_4)}$$

$$L_1(s)=k_1G(s)=\frac{k_1(s+z_1)(s+z_2)(s+z_3)}{(s+p_1)(s+p_2)(s+p_3)(s+p_4)} \quad \text{(a)}$$

$$L_1(j\omega)=\frac{k_1(j\omega+z_1)(j\omega+z_2)(j\omega+z_3)}{(j\omega+p_1)(j\omega+p_2)(j\omega+p_3)(j\omega+p_4)}$$

$$\arg\left(L_1(j\omega)\right)=-180^\circ+PM$$

$$\left|L_1(j\omega_{pm1})\right|=1$$

The last relationship can be used to determine ω_{pm1}

$$\arctan\left(\frac{\omega_{pm1}}{z_1}\right)+\arctan\left(\frac{\omega_{pm1}}{z_2}\right)+\arctan\left(\frac{\omega_{pm1}}{z_3}\right)-\arctan\left(\frac{\omega_{pm1}}{p_1}\right)$$
$$-\arctan\left(\frac{\omega_{pm1}}{p_2}\right)-\arctan\left(\frac{\omega_{pm1}}{p_3}\right)-\arctan\left(\frac{\omega_{pm1}}{p_4}\right)=-180^{\circ}+PM$$

Using relationship (a), we find k_1 The proportional gain coefficient is therefore:

$$k_p=\lim_{s\to 0}L_1(s)=\lim_{s\to 0}k_1G(s)$$

The transfer function of a PID controller is given by the following formula

$$G_{PID}(s)=k_P+\frac{k_i}{s}+k_d s$$

This function can be used as follows

$$G_{PID}(s)=\frac{k_1(s+z_{Pi})(s+z_{pd})}{s}$$

The coefficient k_i is obtained from the relationship

$$k_i=\lim_{s\to 0}G_{pi}(s)G(s)$$

and

$$G_{pi}(s)=\frac{k_1(s+z_{pi})}{s}$$

and

$$k_d=\lim_{s\to 0}G_{pid}(s)G(s)$$

The above method is an algorithm to determine the coefficient of PID regulator.

In this part we present the equations governing the behaviour of the quadratic boost converter, taking into account the active and deactive states [4].

3.1. Continuous Conduction Mode Switch ON

When the "S" switch is activated, we are in the time interval [t_0, t_{on}].

Figure 4 shows the structure of a quadratic boost when the switch is in active mode.

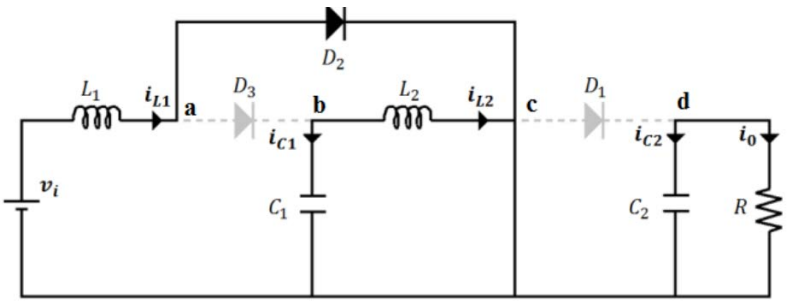


Figure 4. Basic diagram of quadratic boost converter in activated mode.

The current flowing through L_1 forces the conduction of diode D_2 while diodes D_1 and D_3 are blocked. In this mode, the two inductors L_1 and L_2 are charged by the input voltage V_i and V_{c1} respectively, I_{L1} and I_{L2} increase from $I_{\min}$ to $I_{\max}$. The charging current i_0 is supplied by capacitor C_2 [5].

The differential equations for the state variables are as follows when the switch is closed.

$$\Delta iL_1 = \frac{V_i}{L_1} \tag{1}$$

$$\Delta iL_2 = \frac{V_{C1}}{L_2} \tag{2}$$

$$\Delta VC_1 = -\frac{i_{L2}}{C_1} \tag{3}$$

$$\Delta VC_2 = -\frac{V_{out}}{RC_2} \tag{4}$$

iL_1 and ΔiL_2 are the current variations respectively at inductors L_1 and L_2 and ΔVC_1 and ΔVC_2 those of the voltages across C_1 and C_2. ΔiL_1 and ΔiL_2 are the current variations respectively at inductances L_1 and L_2 and ΔVC_1 and ΔVC_2 those of the voltages across C_1 and C_2.

3.2. Continuous Conduction Mode Switch S Deactivate OFF

We have the configuration in Figure 5 when the transistor is disabled.

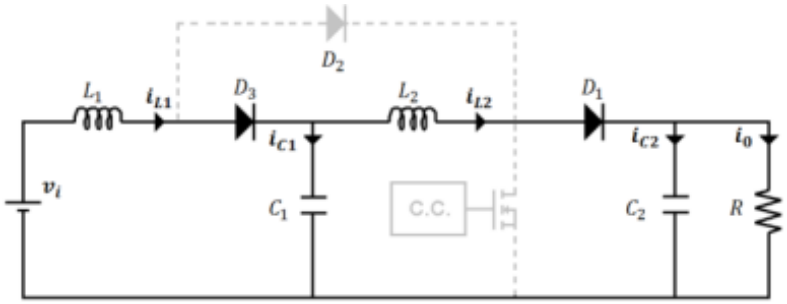


Figure 5. Basic diagram of quadratic boost converter in deactivated mode.

The Diode D_2 is now non-transient while diodes D_1 and D_3 are transient, allowing current to flow through the inductors to charge capacitors C_1 and C_2.

The differential equations relating the state variables when switch S is off are [6]:

$$\Delta iL_1 = \frac{V_i}{L_1} - \frac{V_{C1}}{L_1} \tag{5}$$

$$\Delta iL_2 = \frac{V_{C1}}{L_2} - \frac{V_{out}}{L_2} \tag{6}$$

$$\Delta VC_1 = \frac{i_{L1}}{C_1} - \frac{i_{L2}}{C_1} \tag{7}$$

$$V_{out} = \frac{i_{L2}}{C_2} - \frac{V_{out}}{RC_2} \tag{8}$$

For switching converters, average values are used. We have the following equations:

$$\Delta iL_1 = \frac{V_i}{L_1} - \frac{V_{C1}}{L_1}(1-D) \tag{9}$$

$$\Delta iL_2 = \frac{V_{C1}}{L_2} - \frac{V_{out}}{L_2}(1-D) \tag{10}$$

$$\Delta VC_1 = \frac{i_{L1}}{C_1}(1-D) - \frac{i_{L2}}{C_1} \tag{11}$$

$$\Delta V_{out} = \frac{i_{L2}}{C_2} - \frac{V_{out}}{RC_2} \tag{12}$$

In steady state, the sum of the voltages for a switching operation must be equal to zero. We therefore have:

For the inductance L_1

$$\Delta iL_{1(ON)} + \Delta iL_{1(OFF)} = 0 \tag{13}$$

$$V_{C1} = \frac{V_i}{1-D} \tag{14}$$

For the inductance L_2

$$\Delta iL_{2(ON)} + \Delta iL_{2(OFF)} = 0 \tag{15}$$

$$V_{out} = \frac{V_i}{(1-D)^2} \tag{16}$$

For the currents we have:

$$i_{C(ON)} + i_{C(OFF)} = 0 \tag{17}$$

$$iL_2 = \frac{i_0}{1-D} \quad \text{and} \quad iL_1 = \frac{i_0}{(1-D)^2} \tag{18}$$

The mathematical model and its behaviour are studied. We will now move on to the dimensioning of these components.

The sizing requires knowledge of the coefficients of the transfer function of the system studied.

The electrical components for the design of quadratic boost can be sized from the following relationships [7]:

To determine the self L_1 we have:

$$L_1 = \frac{V_{out}(1-D)^2 D}{\Delta iL_1 f} \quad \text{and} \quad L_2 = \frac{V_{out}(1-D)D}{\Delta iL_2 f} \tag{19}$$

To determine the capacity, we have:

$$C_1 = \frac{D * i_0}{(1-D) f \Delta V C_1} \quad \text{and} \quad C_2 = \frac{D * i_0}{f * \Delta V C_2} \tag{20}$$

In this article we take as input voltage V_i the value 17 V, output voltage V_{out} equal to 250 V and the load of the resistance 100 Ω. The switching frequency of the transistors is set at 100 KHz [8].

The values of the components are given in Table 1.

Table 1. Values of the components of the boost quadratic converter.

Parameters	Values
Input voltage E	17 V
Output voltage V_0	250 V
Duty cycle D	0.74
Inductor L_1	625 µH
Inductor L_2	2.4 mH
capacitor C_1	355 µF
capacitor C_2	92 µF
Switching frequency	100 KHz
Load	100 Ω

4. Results and Discussions

We present in this part the signals obtained from our device (control, power transistor), as well as the results obtained. Figure 6 is an actual photo of the quadratic boost converter.

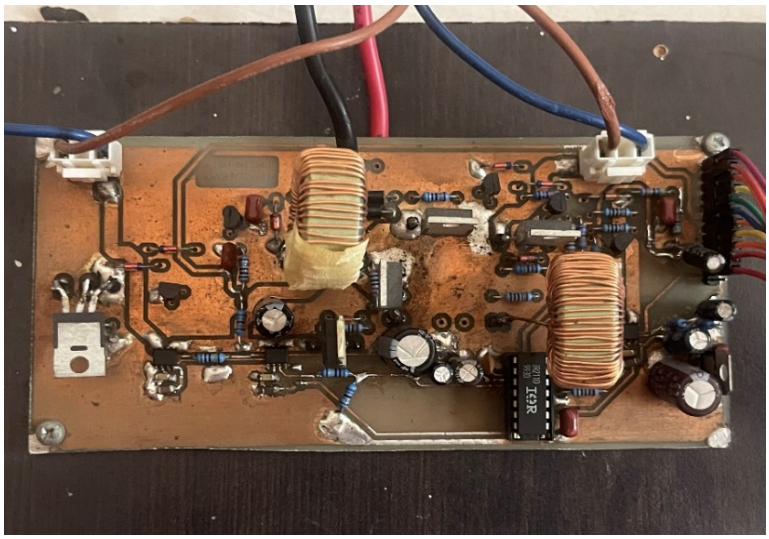


Figure 6. Photo of quadratic boost converter.

4.1. Variation of Output Voltage as a Function of Duty Cycle

In the following, we present the evolution of the output voltage of the DC-DC converter as a function of the duty cycle. The aim is to highlight the effects, *i.e.*

the influence of the input voltage and the influence of the load.

4.1.1. Effect of Load

We study the evolution of the output voltage as a function of the duty cycle under the effect of the load, as shown in Figure 7.

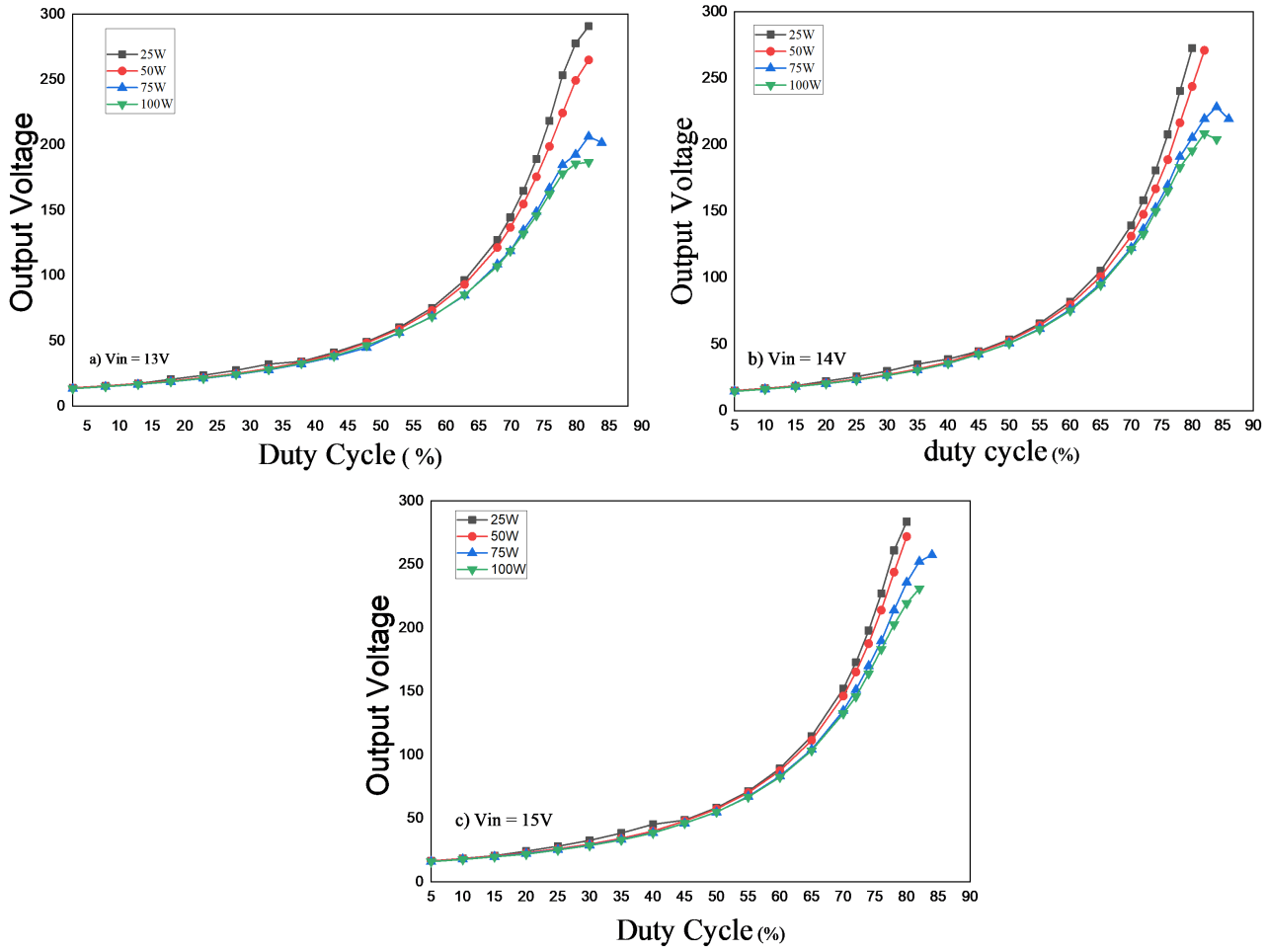


Figure 7. Variation in output voltage as a function of duty cycle.

The output voltage increases with the duty cycle until it reaches a limit at which it begins to drop. This part corresponds to the increase in losses in the converter, which explains the drop observed.

For a given duty cycle, the higher the load, the lower the voltage obtained. As the duty cycle increases, the imperfections of the various components (inductor, capacitor and transistor) become apparent, leading to the decreases observed.

4.1.2. Influence of the Input Voltage

We now present the evolution of the output voltage as a function of the duty cycle for different voltages at the input of the converter (Figure 8), for given loads.

Contrary to the effect of the load, the output voltage increases with the input voltage.

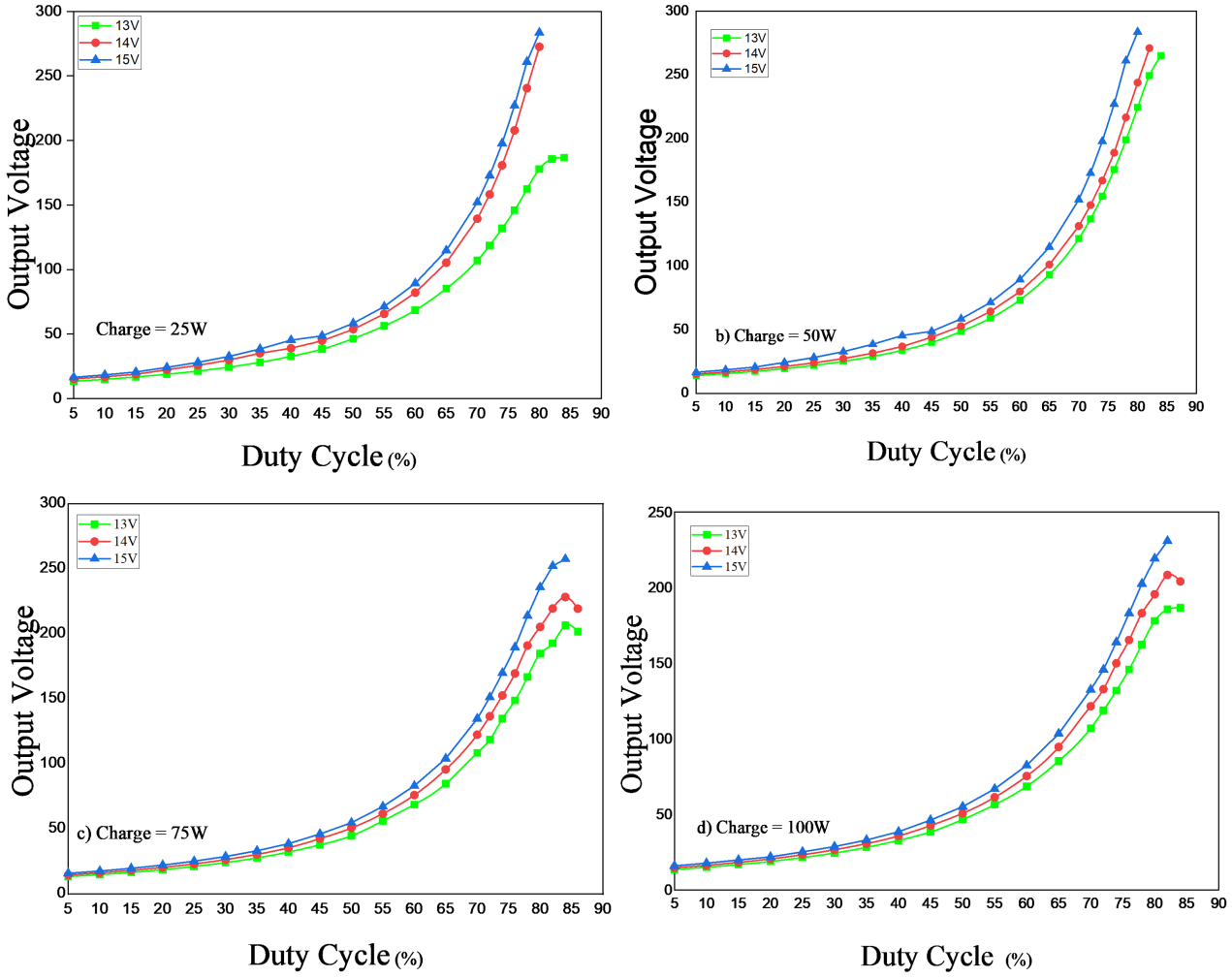


Figure 8. Variation of output voltages as a function of duty cycle.

This increase is all the greater if the load is low. However, for high duty cycles, there is a limit beyond which the voltage begins to decrease, and this is essentially due to losses in the DC-DC converter.

4.2. Variation of Output Power as a Function of Duty Cycle

In this part, we study the evolution of the output power as a function of the duty cycle under the effect of the load and under the effect of the input voltage.

4.2.1. Effect of Load

In this paragraph, we present the influence of the DC-DC converter output power as a function of the duty cycle for different load values (**Figure 9**).

There is an increasing trend in output power as a function of the duty cycle. This trend is all the more significant for duty cycles above 70%. However, there is a limit value for the duty cycle, around 80%, beyond which the output power decreases. This decrease is due to overheating of the transistors, leading to losses due to the Joule effect.

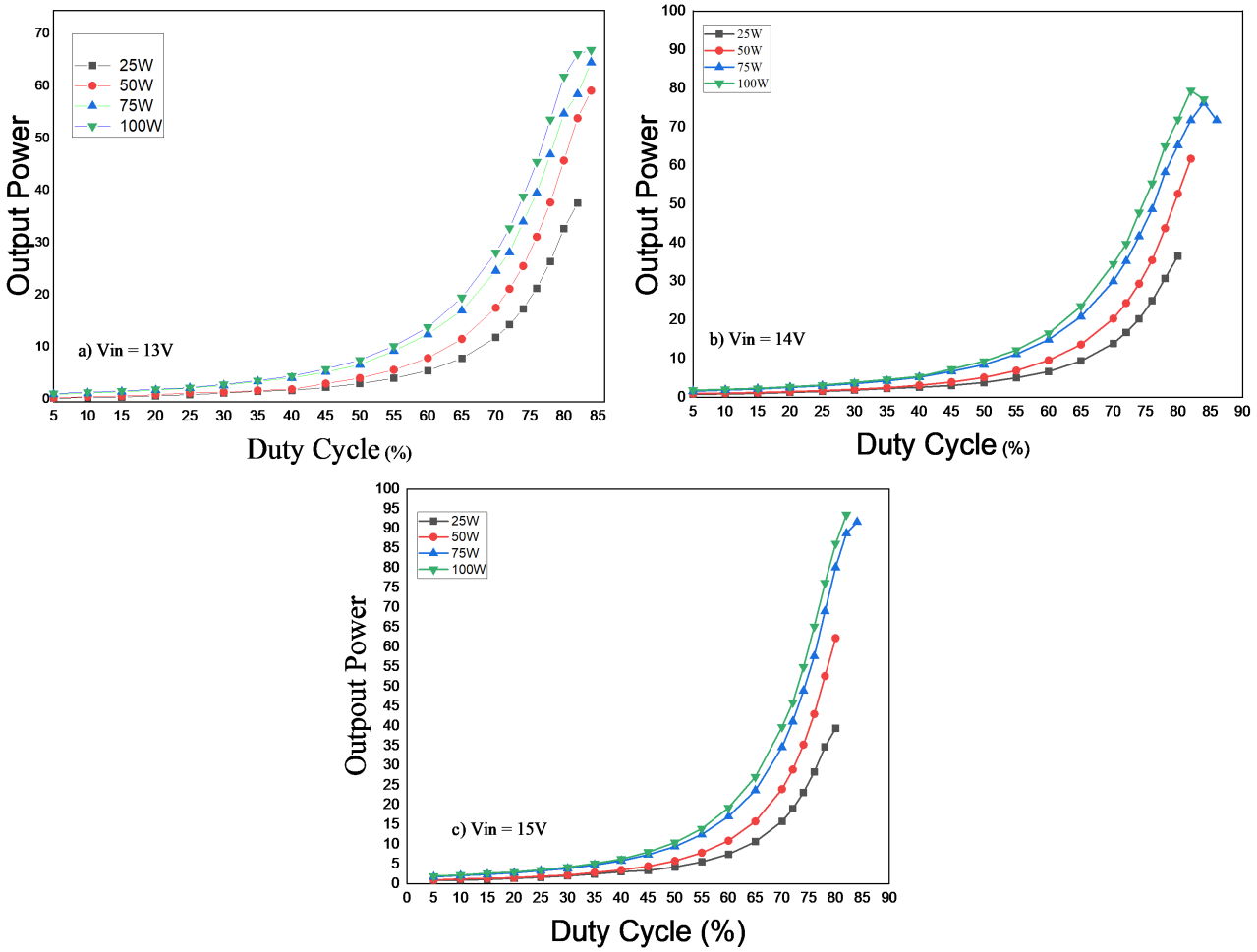
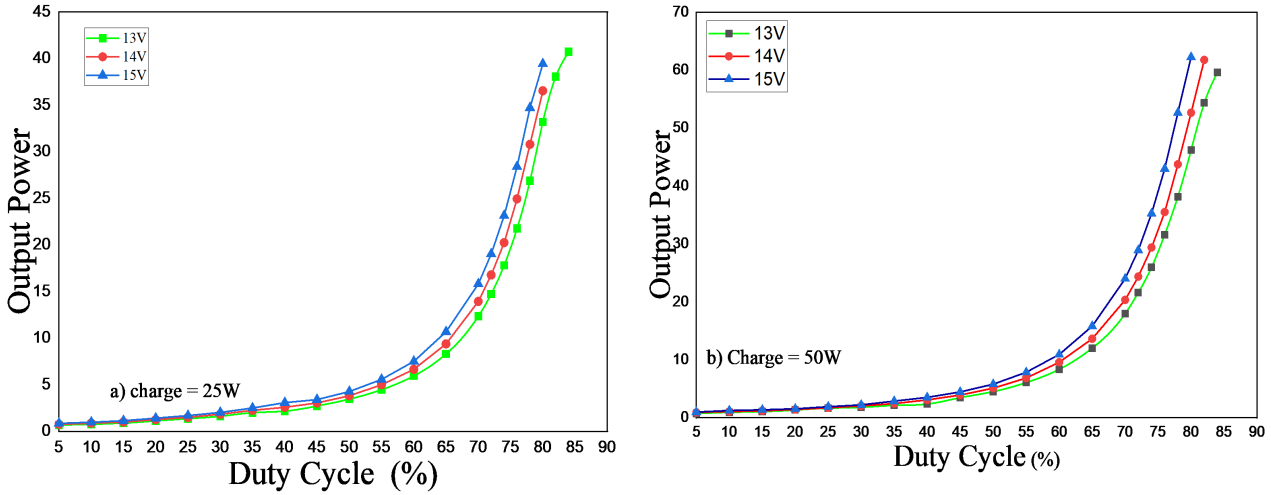


Figure 9. Variation in output power as a function of duty cycle.

4.2.2. Effect of Input Voltage

In this part, we want to show the variation in output power as a function of the duty cycle under the influence of the input voltage (**Figure 10**).



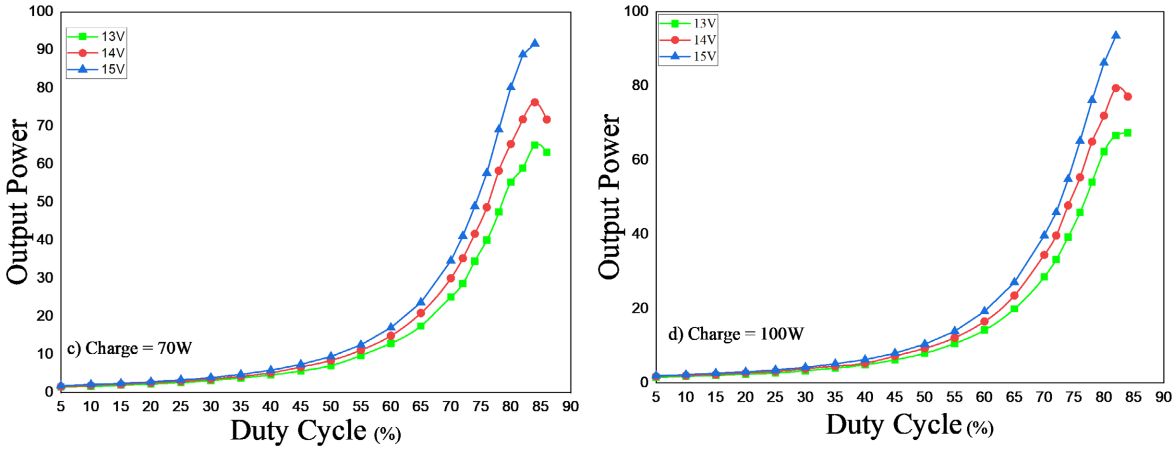


Figure 10. Variation in output power as a function of duty cycle.

The variations in output power as a function of duty cycle for nominal voltages are shown in Figure 10. These curves show that the output power increases with the duty cycle. Obviously, the higher the input voltage, the higher the output power.

4.3. Conversion Efficiency as a Function of Duty Cycle

The aim of this section is to study the variation in conversion efficiency under the effect of load and under the effect of input voltage. This will enable us to determine the efficiency of our system and its robustness.

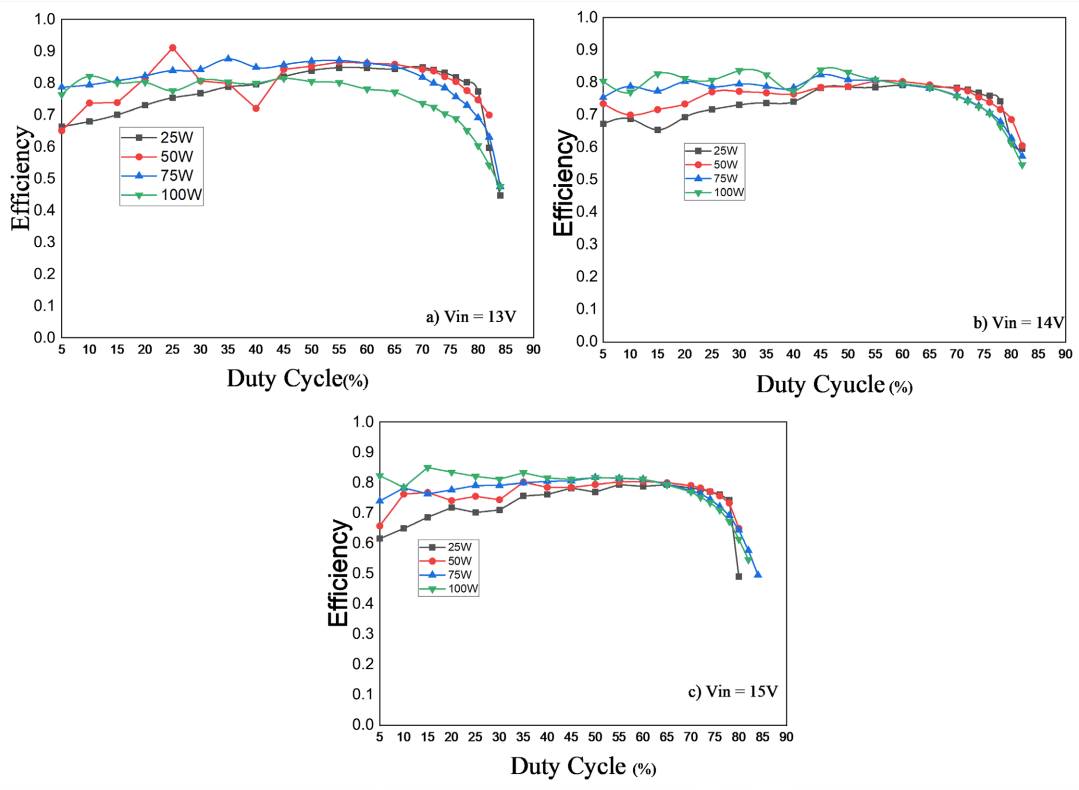


Figure 11. Variation in efficiency as a function of duty cycle.

4.3.1. Effect of Load

In this section, we present Figure 11 the conversion efficiency, *i.e.* the ratio of output power to input power as a function of the duty cycle under load.

The efficiency curves as a function of duty cycle under the influence of load show two phases. The first phase lies between duty cycles of 5% and 70%. During this interval there is a slight variation in efficiency with 60% and 80%.

The second phase begins when the cyclical ratio exceeds 70%. During this phase we notice a drop in efficiency. This drop is due to switching losses in the transistors linked to the voltage drops generated by the inductors.

4.3.2. Influence of Input Voltage

In this part of our presentation, we show the evolution of the efficiency as a function of the duty cycle for different input voltages (Figure 12).

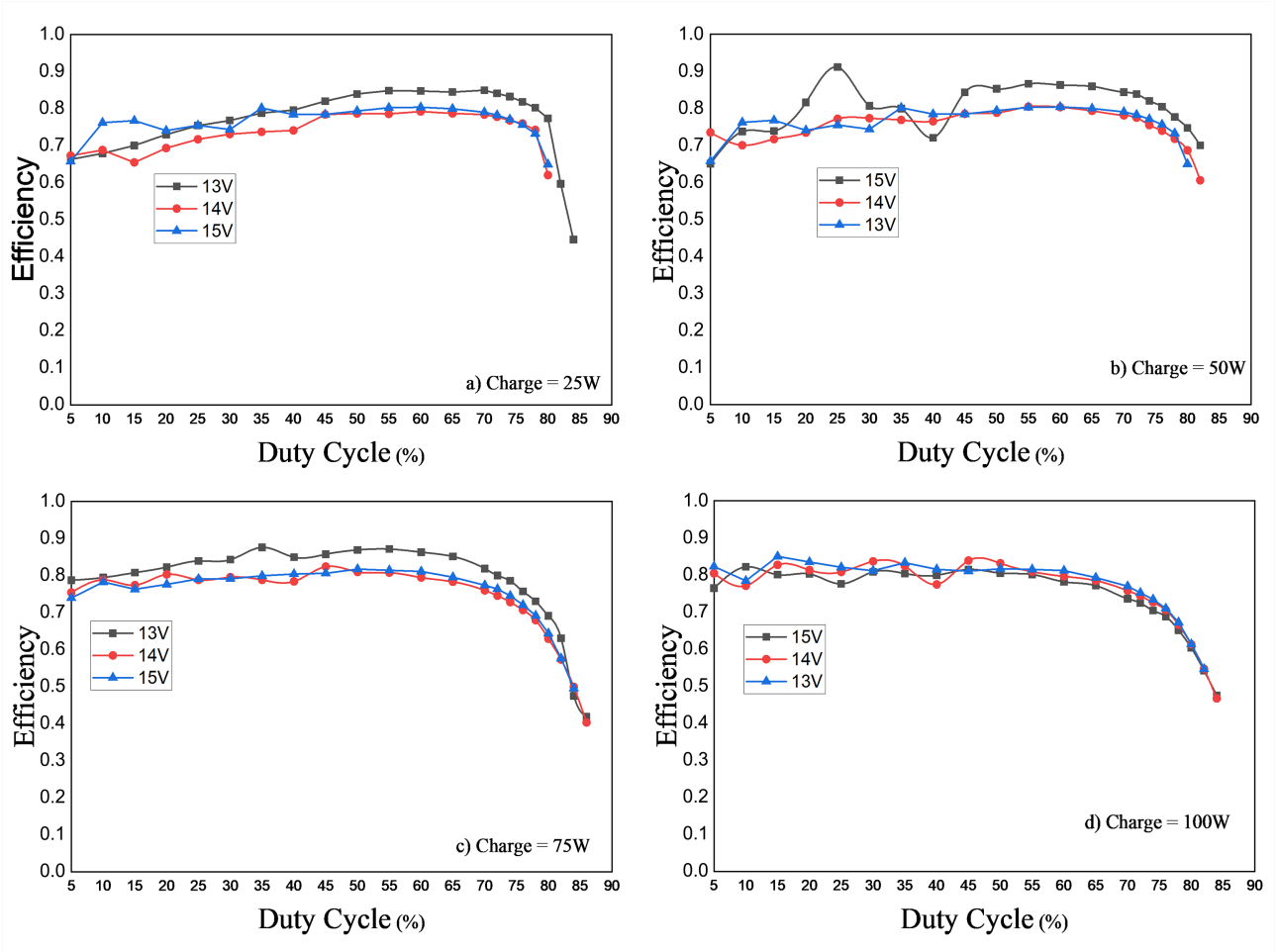


Figure 12. Converter efficiency versus duty cycle.

We can see that the higher the input voltage, the higher the efficiency. There is also an increase in the efficiency value compared with the influence of the load, as we obtained values between 75% and 90%. However, there is a drop in efficiency when the duty cycle is greater than 75%. This drop is all the greater at higher loads.

5. Comparison between Actual Performance and Theoretical Performance

In reading this section, we will compare the yield curves obtained theoretically with those obtained from actual measurements. This will enable us to confirm or invalidate the practical work we have already done.

The yield expression obtained from the quadratic boost modelling is given by the following relationship [9]:

$$\eta = \frac{1}{1+\left[\dfrac{\alpha(1-\alpha)r_{c_1}+r_{L_1}}{(1-\alpha)^4 R}+\dfrac{\alpha(1-\alpha)r_{c_2}+r_{L_2}}{(1-\alpha)^2 R}\right]} \tag{21}$$

where $\alpha, r_{c_1}, r_{L_1}, r_{c_2}, r_{L_2}, R$ are the coefficients, representing respectively the duty cycle, the resistances of capacitor C_1, inductance L_1, capacitor C_2, inductance L_2 and load R.

In what follows, we will present a comparative study between the theoretical model and the real model (Figure 13).

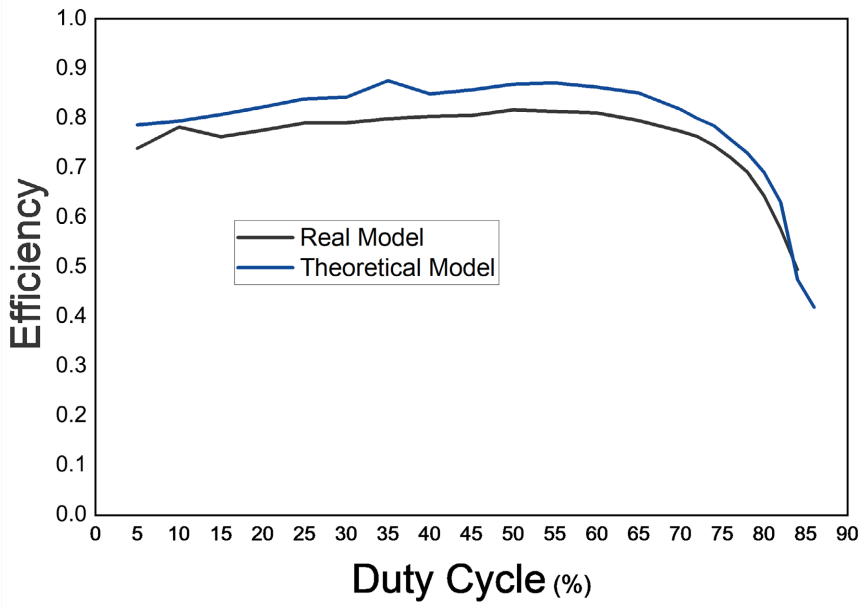


Figure 13. Comparison curves between the real model and the theoretical model.

Superimposing the two models, theoretical (blue curve) and real (black curve) reveals a homogeneity in terms of evolution. We can therefore deduce that our measurements are in line with reality.

6. Conclusion

In this paper, we first present the structure of a quadratic boost converter and its various operating modes. We then proceeded to the dimensioning of its components with a view to its practical implementation. Once the design was complete, we supplemented our study with a theoretical study in order to validate our work.

We also carried out a series of tests followed by data analysis to determine its conversion efficiency. We would like to continue our work by adding a second stage that will handle DC-AC conversion in a future paper.

Conflicts of Interest

The authors declare no conflicts of interest regarding the publication of this paper.

References

[1] Lopez-Santos, O., Martinez-Salamero, L., Garcia, G., Valderrama-Blavi, H. and Sierra-Polanco, T. (2013) Comparison of Quadratic Boost Topologies Operating under Sliding-Mode Control. 2013 *Brazilian Power Electronics Conference*, Gramado, 27-31 October 2013, 66-71. https://doi.org/10.1109/cobep.2013.6785096

[2] Forouzesh, M., Siwakoti, Y.P., Gorji, S.A., Blaabjerg, F. and Lehman, B. (2017) Step-up DC-DC Converters: A Comprehensive Review of Voltage-Boosting Techniques, Topologies, and Applications. *IEEE Transactions on Power Electronics*, **32**, 9143-9178. https://doi.org/10.1109/tpel.2017.2652318

[3] Prabha, B.S. and Ramprasath, M.S. (2018) Mathematical Modelling and Performance Analysis of Quadratic Boost Converter. *International Journal of Scientific & Engineering Research*, **9**, 190-196.

[4] Sivaraj, D. and Arounassalame, M. (2017) Control of Quadratic Boost Converter Using Fractional Order PID Controller. 2017 *Innovations in Power and Advanced Computing Technologies* (*i-PACT*), Vellore, 21-22 April 2017, 1-6. https://doi.org/10.1109/ipact.2017.8244979

[5] Alghaythi, M.L., O'Connell, R.M., Islam, N.E., Khan, M.M.S. and Guerrero, J.M. (2020) A High Step-Up Interleaved DC-DC Converter with Voltage Multiplier and Coupled Inductors for Renewable Energy Systems. *IEEE Access*, **8**, 123165-123174. https://doi.org/10.1109/access.2020.3007137

[6] Choudhury, T.R. and Nayak, B. (2015) Comparison and Analysis of Cascaded and Quadratic Boost Converter. 2015 *IEEE Power*, *Communication and Information Technology Conference* (*PCITC*), Bhubaneswar, 15-17 October 2015, 78-83. https://doi.org/10.1109/pcitc.2015.7438108

[7] Tattiwong, K. and Bunlaksananusorn, C. (2014) Analysis Design and Experimental Verification of a Quadratic Boost Converter. *TENCON* 2014—2014 *IEEE Region* 10 *Conference*, Bangkok, 22-25 October 2014, 1-6. https://doi.org/10.1109/tencon.2014.7022467

[8] Badiane, M., Honadia, P.A.A., Zouma, B. and Barro, F.I. (2021) Quadratic Boost Converter: An Analysis with Passive Components Losses. *Open Journal of Applied Sciences*, **11**, 202-215. https://doi.org/10.4236/ojapps.2021.112014

[9] Badiane, M., Honadia, P.A.A. and Barro, F.I. (2020) Theoretical and Experimental Analysis of a Boost Converter. *Journal de Physique de la Soaphys*, **2**, C20A28-1-C20A28-9.