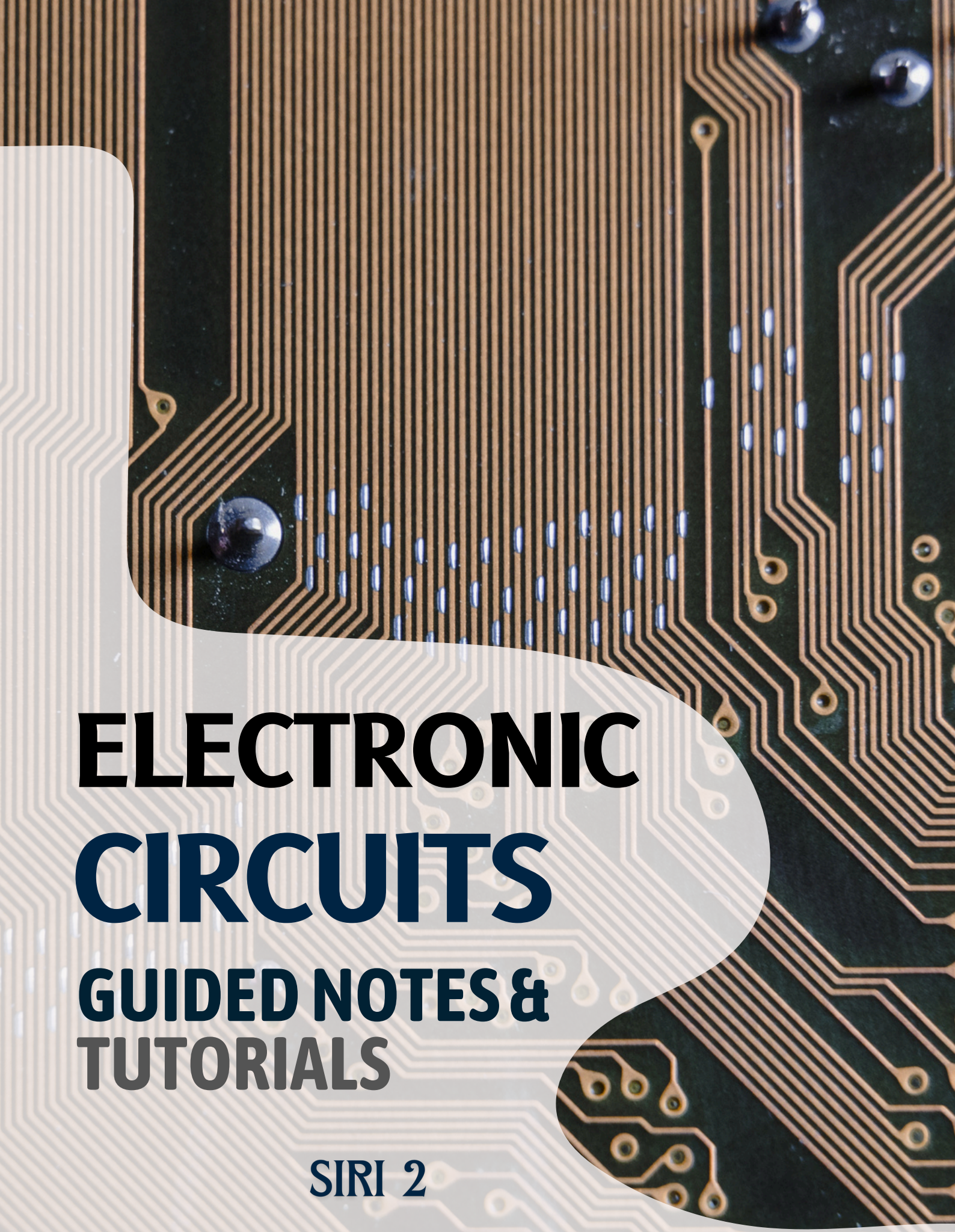

ELECTRONIC CIRCUITS

GUIDED NOTES & TUTORIALS

SIRI 2

ELECTRONIC CIRCUITS

GUIDED NOTES & TUTORIALS

SIRI 2

TIMERS – FILTERS – ANALOGUE/DIGITAL CONVERTERS

MOHD FARIZUL IRNI BIN ISMAIL

ROHAILA BINTI MOHD RADI

MIRDAA BINTI MAZNOR

POLITEKNIK MALAYSIA
PORT DICKSON

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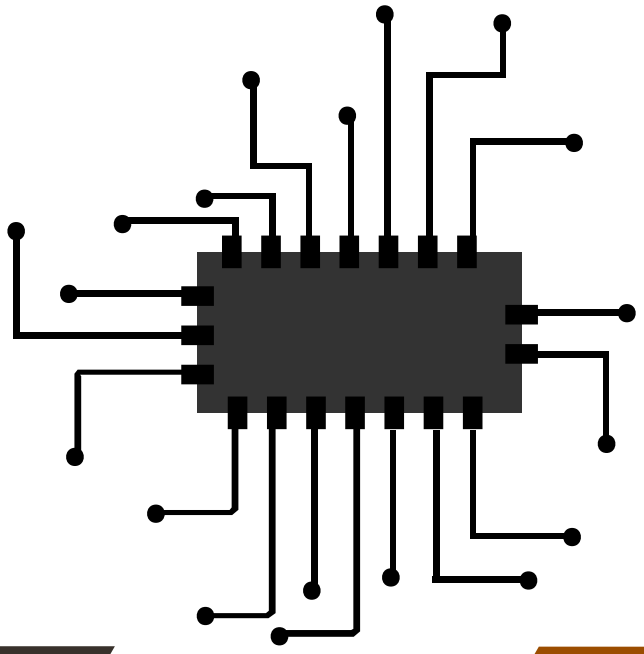
PREFACE

An electronic circuit book is a comprehensive resource designed to facilitate the study of topics such as Timers, Filters and Analogue/Digital Converters.

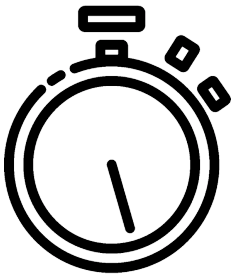
It includes a range of exercises and tutorials for each subject area, aimed at enhancing the reader's understanding of the concepts and foundational principles covered in the course. Moreover, the book is presented in a more engaging writing style to enrich the educational experience.

TABLE OF CONTENTS



TIMERS

SCAN HERE



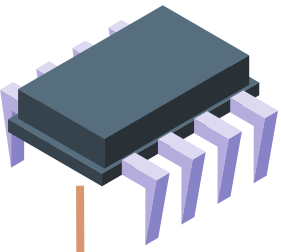
WHAT IS TIMER?

A timer is a specialized type of clock.

Timer can used to measure and control the passage of time.

Timers can be mechanical, electromechanical, electronic or even software as all modern computers include digital timers.

Timer can be set to trigger an event or signal after a specific interval, or to count time up or down depending on the application.

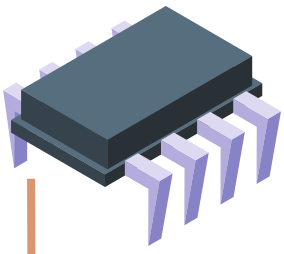


IC TIMER 555

- The 555 timer is an integrated circuit specifically used for generating time delays, pulses, and oscillations.
- Timer also designed to perform signal generation (such as a simple pulse or continuous square wave), timing functions.
- IC NE/SE 555 is a highly stable device for generating accurate time delays.
- Commercially, this IC is available in 8-pin circular

Basic Features :

Supply voltage: 4.5V to 15V
Output current: Up to 200 mA
Adjustable duty cycle and frequency
Stable temperature performance
Compatible with both TTL and CMOS logic families.



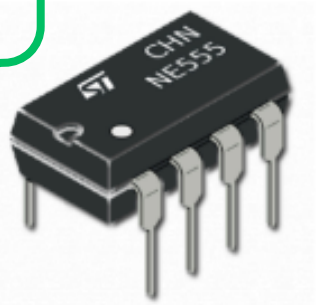
PIN FUNCTION TIMER -555

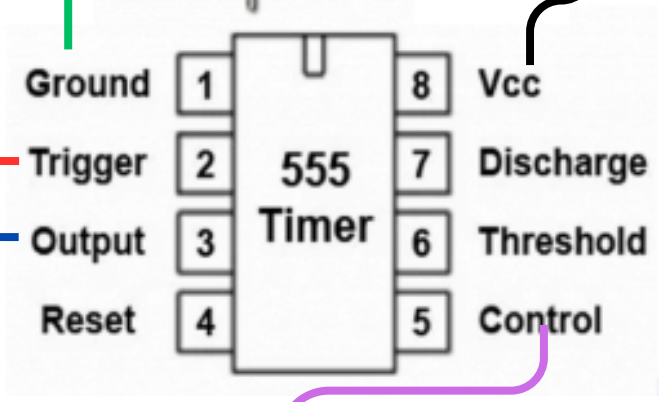
Pin ground where all the measured voltage must be referred to this pin

When the voltage is less than 1/3 Vs (active low), the output becomes high (+Vcc).
It monitors the discharging of the timing capacitor in an astable circuit.
It has a high input impedance of >2MΩ.

The output can be connected to two pins.
The output pins are either pin 3 and pin 1 or pin 3 and pin 8

The threshold voltage is internally set to 2/3 Vcc.
This can be adjusted if needed.
Normally, this function is not used, and the control input is connected to 0V with a 0.01µF capacitor to reduce electrical noise.
If noise isn't an issue, the control input can be left unconnected.





Not an input, listed for convenience.
Connected to 0V when timer output is low.
Used to discharge the timing capacitor in astable and monostable circuits.

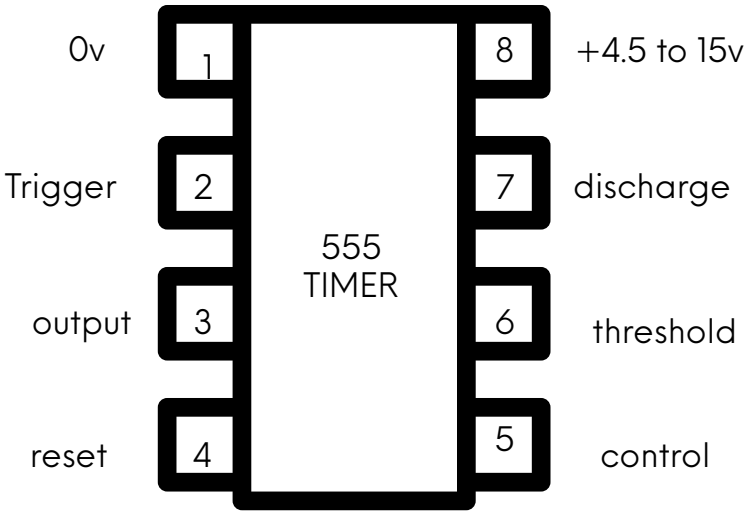
Pin supply + Vcc (+5 v to 18 v)

When the voltage exceeds 2/3 Vcc ('active high'), the output becomes low (0V).
It monitors the charging of the timing capacitor in astable and monostable circuits.
It has a high input impedance (> 10MΩ).
If the trigger input is greater than 1/3 Vcc, the threshold input controls the output.
If the trigger input is less than 1/3 Vcc, it overrides the threshold and holds the output high (+Vcc).

TYPES OF TIMER

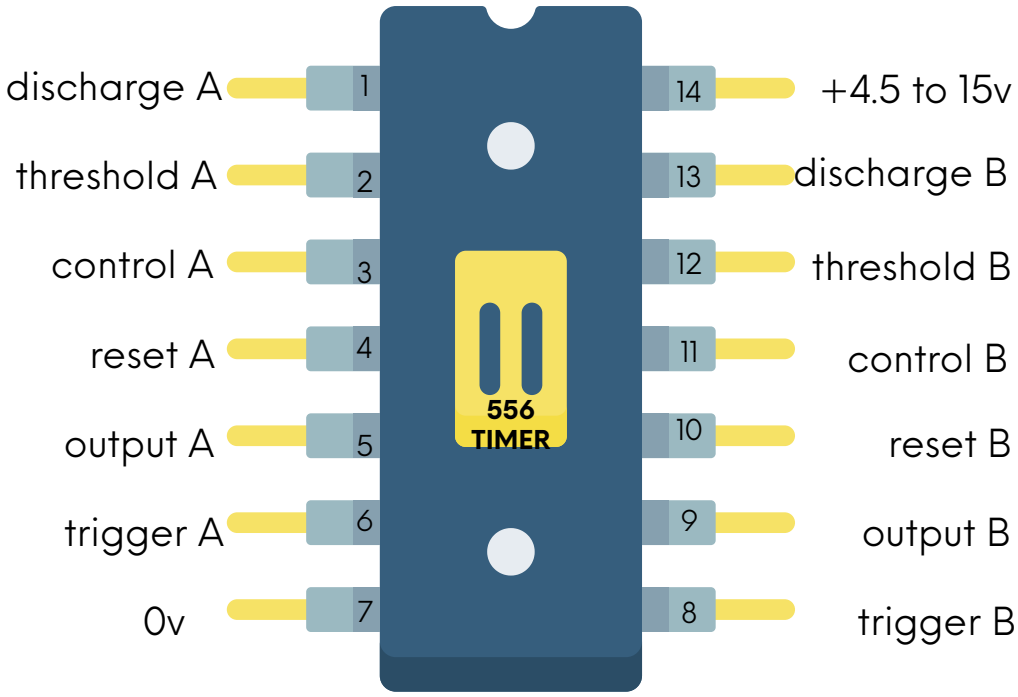
555 Timer

- used in monostable and astable modes.



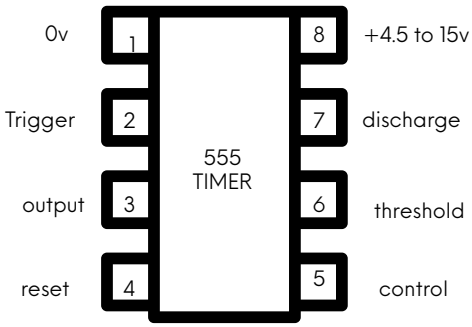
556 Timer

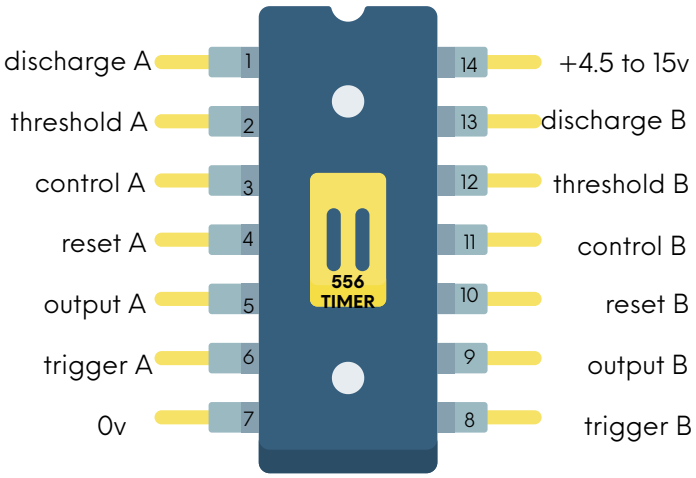
- efficient for compact designs



DUAL TIMER

COMPARISON





DUAL TIMER

- A Popular version is NE 555
- This is suitable in most cases where a '555 timer' is specified.
- 8 pins
- Basic timing functions (monostable, astable, bistable)
- 4.5V to 15V
- One timer block
- Simple circuits (e.g. LED flasher)
- Cheaper and smaller

- The 556 is a dual version of the 555 housed in a 14-pin package,
- The two timers (A and B) share the same power supply pins.
- Two separate timers can run independently or together
- 4.5V to 15V
- Two timer blocks in one chip
- More compact designs needing 2 timers, e.g. delay+trigger
- Slightly more expensive and larger

APPLICATION OF 555 TIMER

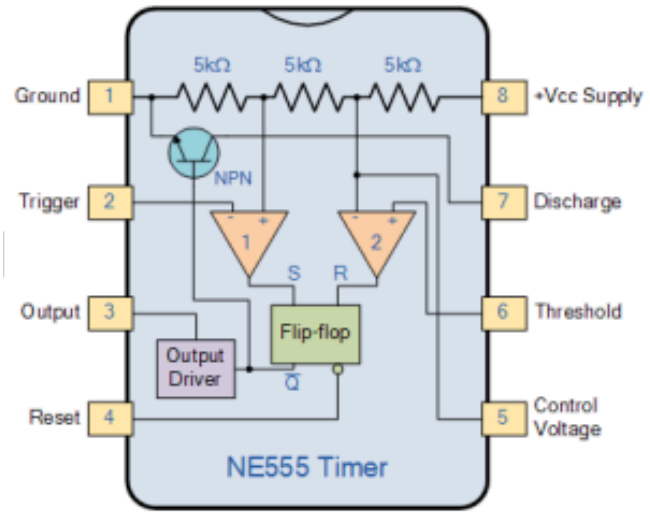
Multivibrator

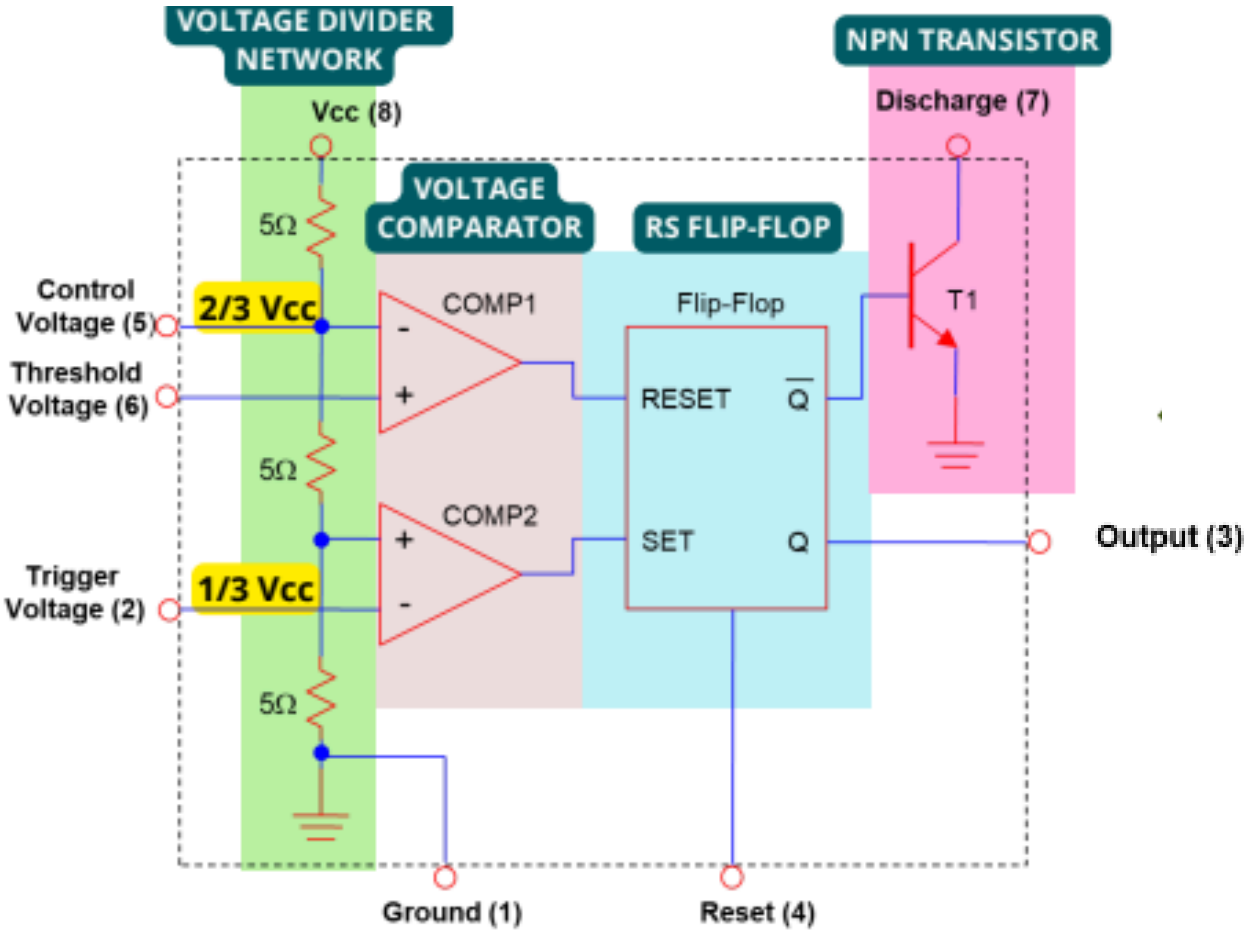
Are a group of regenerative circuits that are used extensively in timing applications. It is a wave shaping circuit which gives symmetric or asymmetric square output

- **Astable Multivibrator**
- **Bistable Multivibrator**
- **Monostable Multivibrator**
- **Schmitt Trigger**

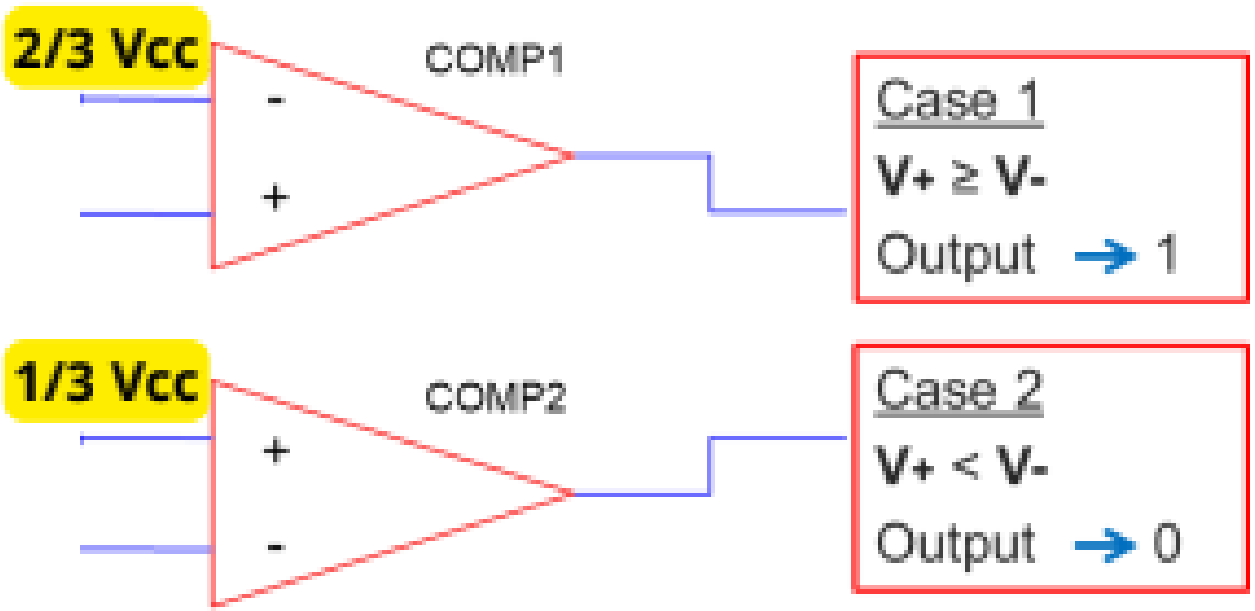
- **Missing Pulse Detector**
- **Linear Ramp Generator**
- **Frequency Divider**
- **Pulse Width Modulation**
- **FSK Generator**
- **Pulse Position Modulator**

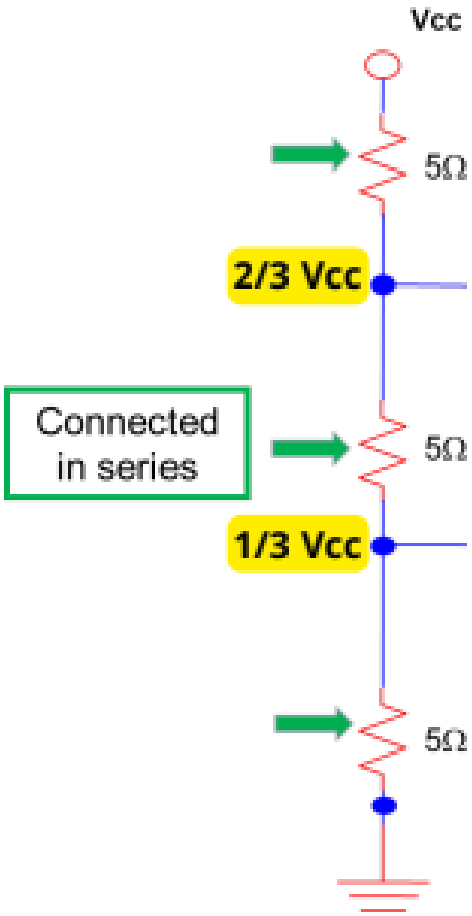
SCHEMATIC BLOCK DIAGRAM TIMER 555





VOLTAGE COMPARATOR

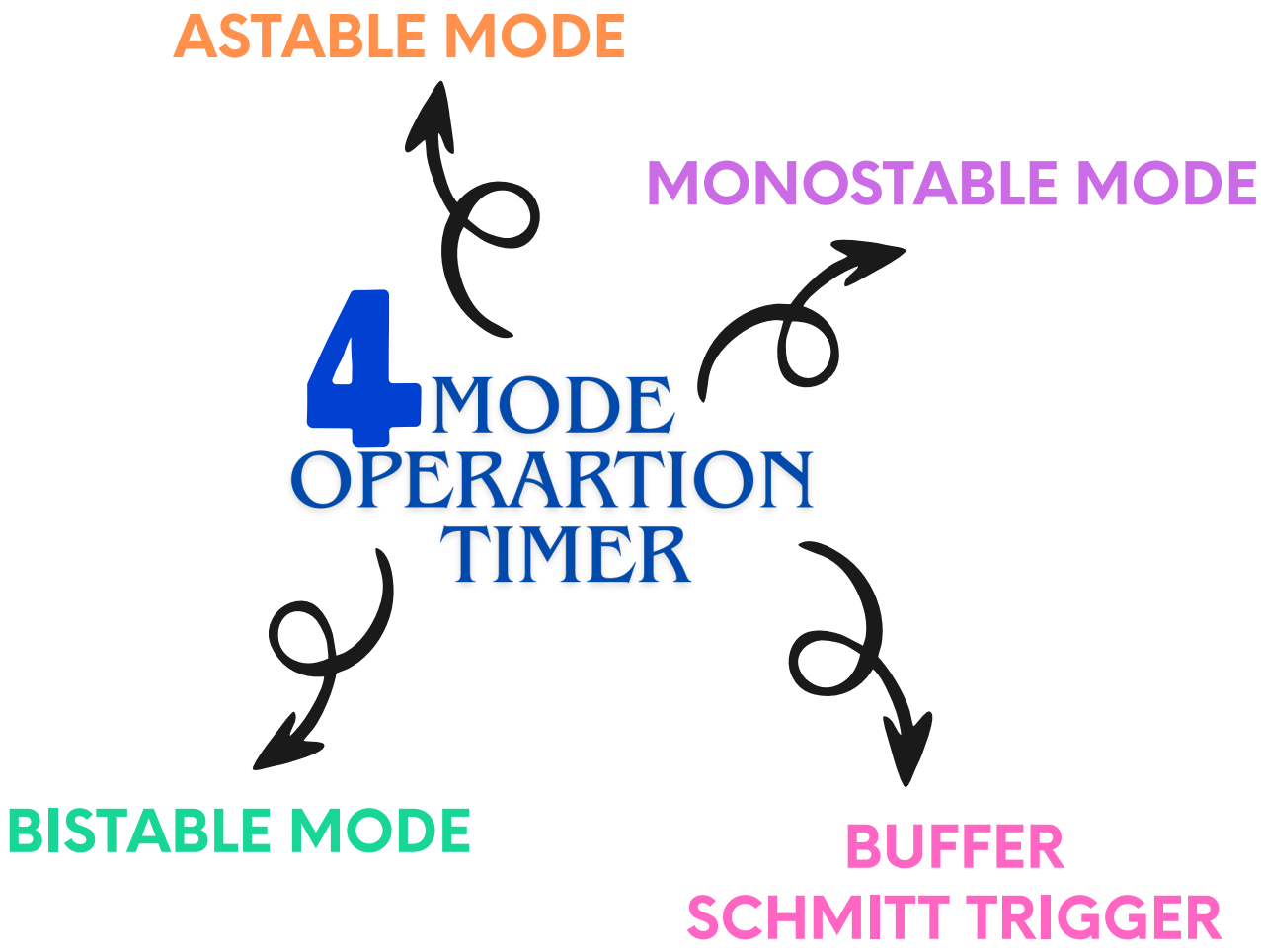




Whenever voltage at non-inverting input (+) is more positive than voltage at inverting input (-) output will be "1" otherwise output will be "0"

MODE OPERATION TIMER

A 555 timer can be configured to operate in four (4) different modes, each suitable for various timing applications.



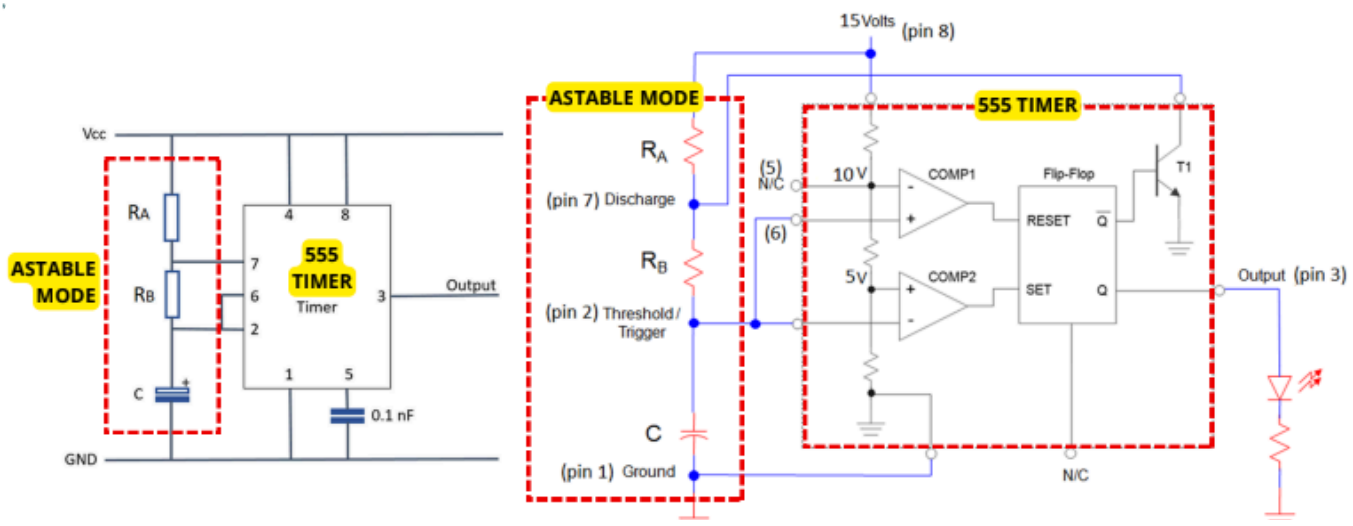
Compare between Astable Mode, Monostable Mode and Bistable Mode

Astable Mode	Monostable Mode	Bistable Mode
Known as one shot multivibrator	Known as Free running multivibrator	Known as Flip Flop
It has only one stable state	There is no stable state	There is stable in two states
Trigger is required for the operation to change the state	Trigger is not required to change the state	No timing involved
Two component R and C are necessary with IC 555 to obtain the circuit	Three components RA, RB and C are necessary with IC 555 to obtain the circuit	-
The frequency of operation is controlled by frequency of trigger pulses applied	The frequency of operation is controlled by RA, RB & C	-
The applications are timer, frequency divider, pulse width modulation	The applications are square wave generator, flasher, voltage controlled oscillator, FSK Generator	The applications are switching and latching circuits, counters, shift registers and primitive memory circuits and also be used in relay control circuit.
Draw Circuit	Draw Circuit	Draw Circuit
T = TH +TL	T + 1.1 (RC)	-

***TIPS**

FINAL QUESTION

SCHEMATIC ASTABLE MODE



$$- \; V_{Comm\,1} : \frac{2}{3} V_{cc} = \frac{2}{3} x \; 15$$

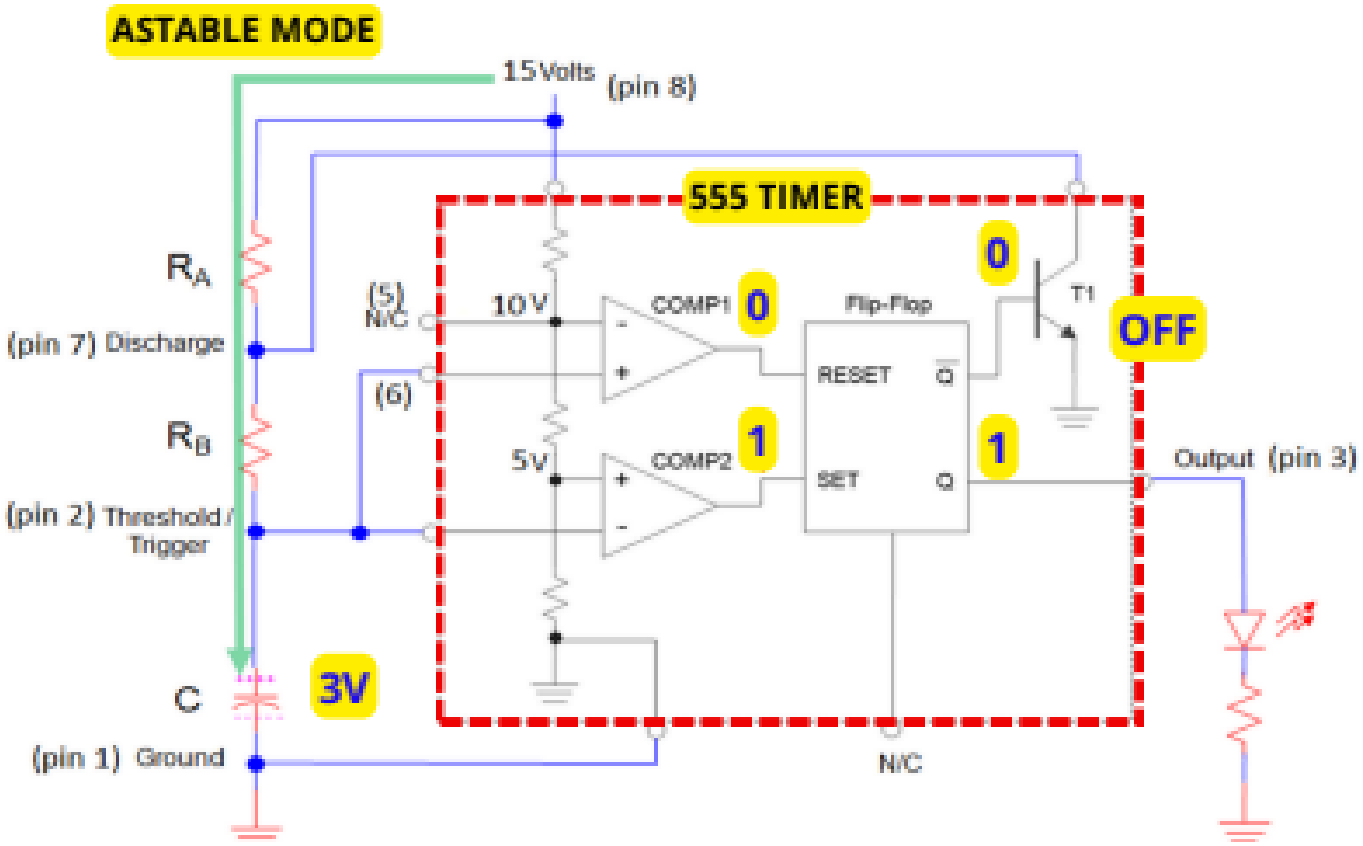
$$= 10 \; V$$

$$+ V_{Comm\,2} : \frac{1}{3} V_{cc} = \frac{1}{3} x \; 15$$

$$= 5 \; V$$

555 Timer Astable Mode

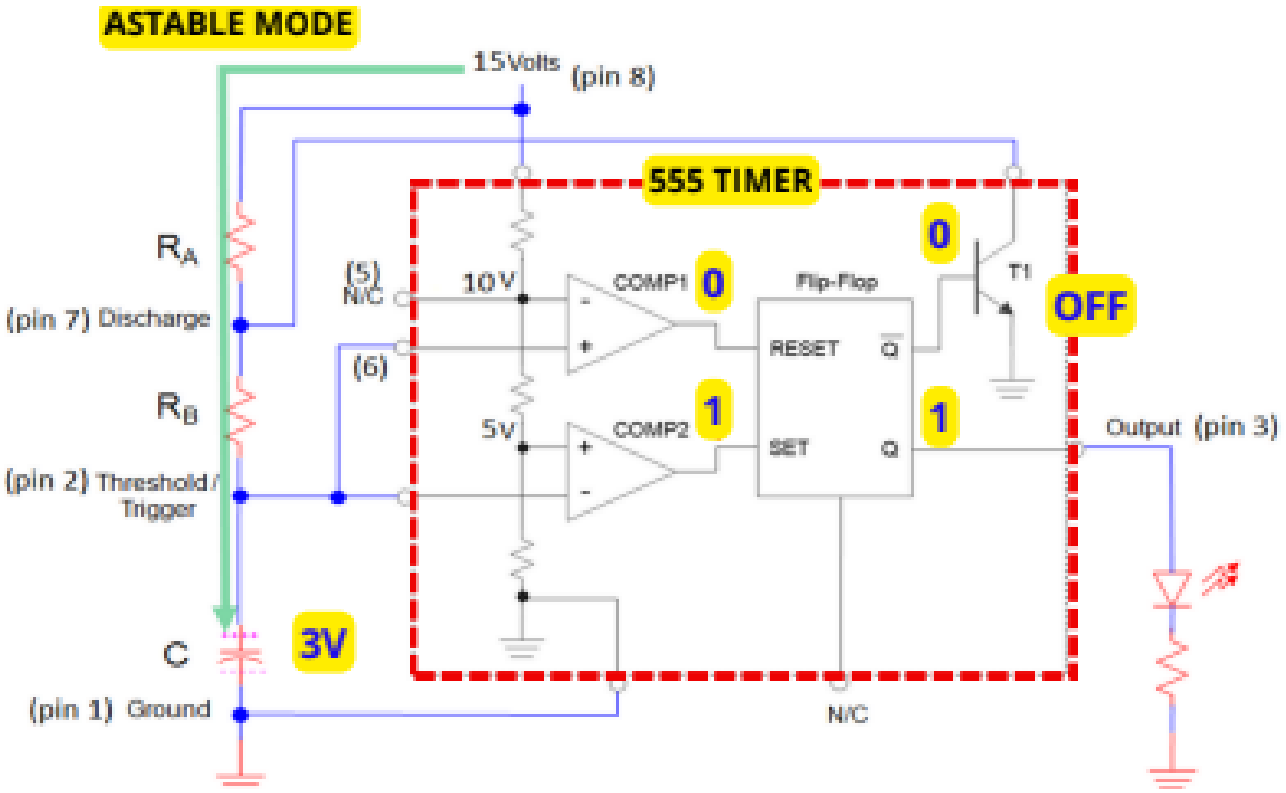
OPERATION OF 555 TIMER IN ASTABLE MODE



- At the moment that **power is applied** to timer, the **capacitor is discharged.**
- Output **Comparator 1** will be **0**, Output **Comparator 2** will be **1**.
- The **output become HIGH** state.
- At this time **T1** is in **OFF** state. Capacitor **C** will **start charging towards the +Vcc via resistors RA and RB.**

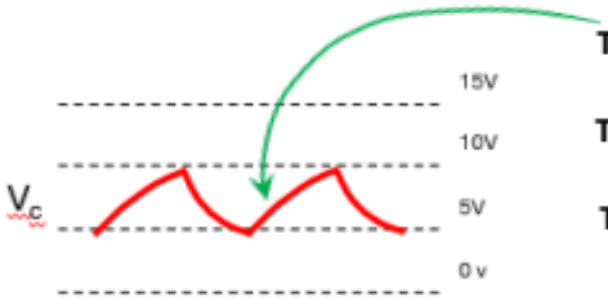
- Capacitor **C charging** towards the **+Vcc** via resistors **RA and RB**. A **voltage build.**
- Output **Comparator 1** still **0**, Output **Comparator 2** still **1.**
- The **output still HIGH** state.
- Capacitor **C continue charging.**

OPERATION OF 555 TIMER IN ASTABLE MODE



- When **capacitor charges to 5V**, Output **Comparator 1** will be **0**, Output **Comparator 2** will be **1**.
- The **output** remain **HIGH** state.
- **Capacitor C continue charging** .

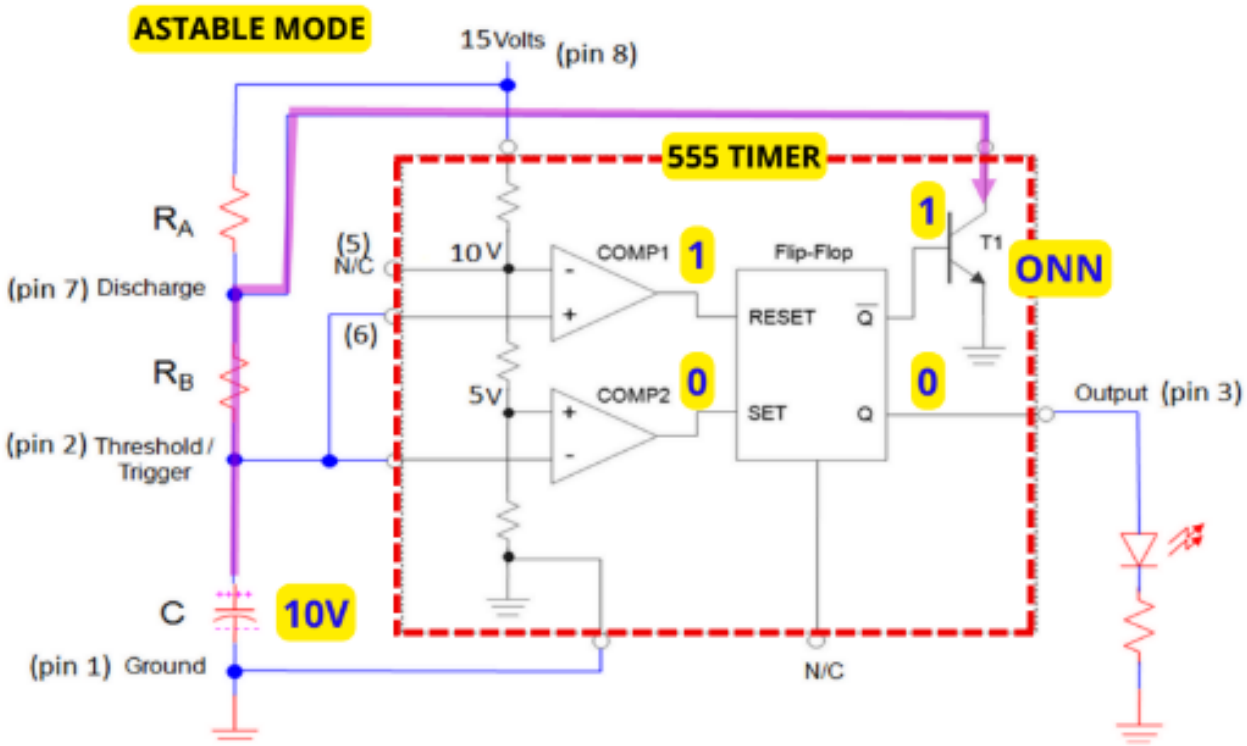
Calculations for the Oscillator's HIGH Time



The Output Is HIGH While The Capacitor Is Charging Through RA + RB.

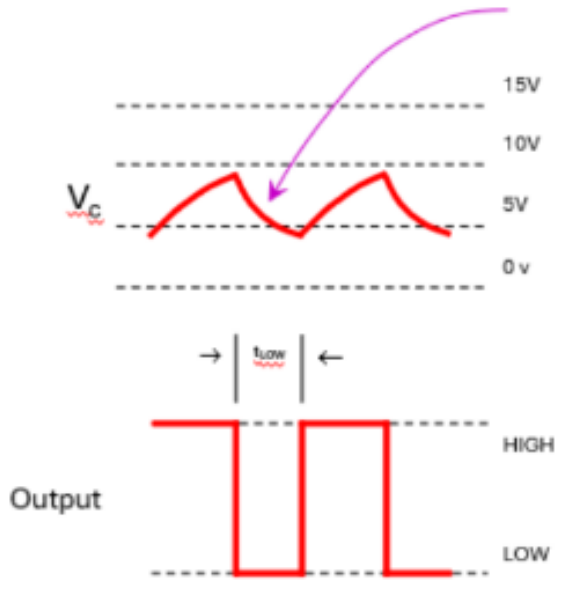
$$t_{HIGH} = 0.693(R_A + R_B)C$$

OPERATION OF 555 TIMER IN ASTABLE MODE



- When **capacitor charges to 10V**, Output **Comparator 1** goes **1**, Output **Comparator 2** still **0**.
- The **output goes LOW** state.
- At this time **T1** is in **ON** state, which **create a path for Capacitor C to discharge**.

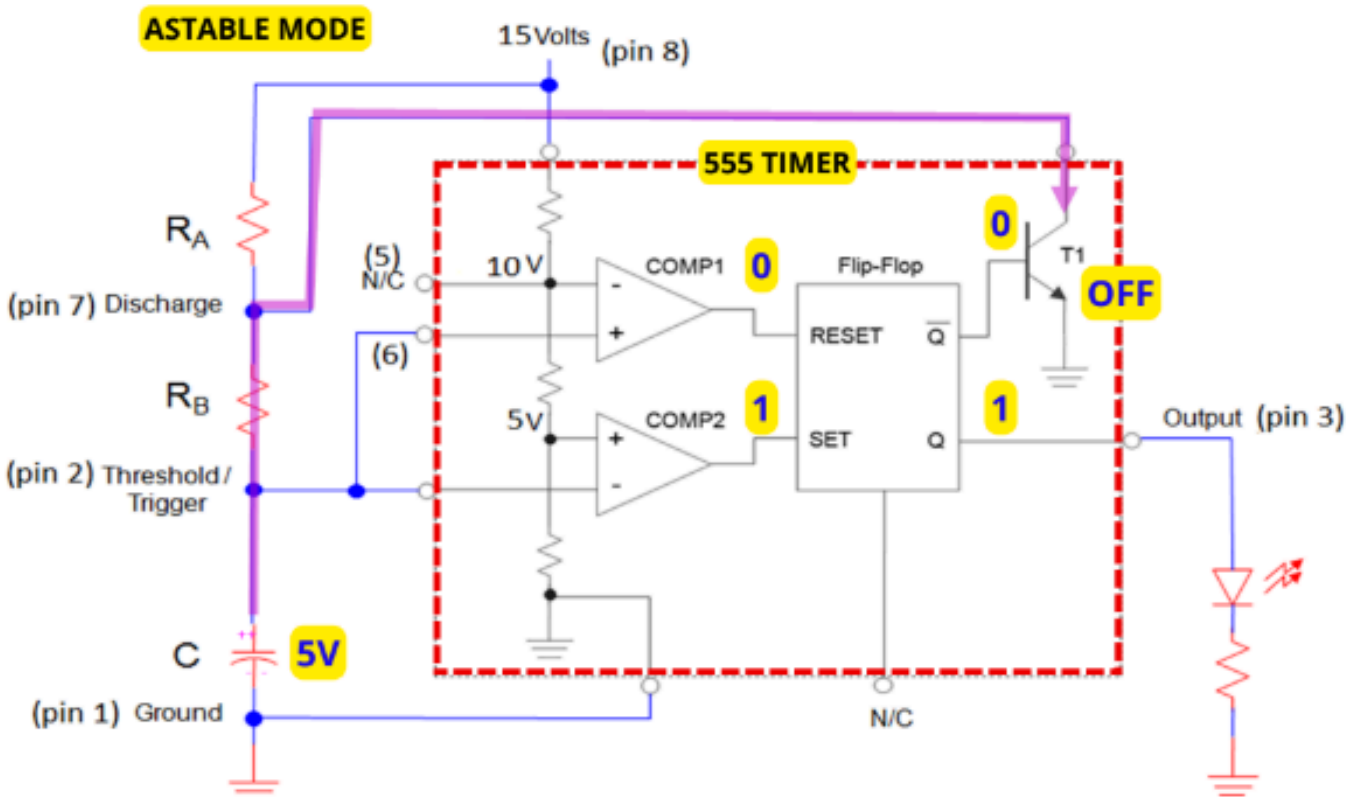
Calculations for the Oscillator's LOW Time



The Output Is LOW While The Capacitor Is Discharging Through RB.

$$t_{LOW} = 0.693 R_B C$$

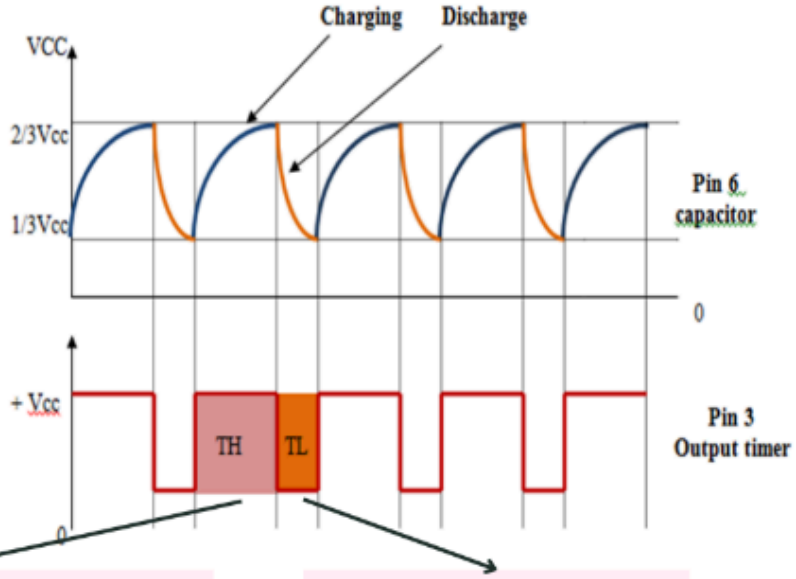
OPERATION OF 555 TIMER IN ASTABLE MODE



- When **capacitor discharges to 5V**, Output **Comparator 1** still **0**, Output **Comparator 2** goes to **1**.
- The **output goes HIGH** state.
- At this time **T1** is in **OFF** state and **open the discharge path**.
- Capacitor **C begin to charges again**. The count will be repeated.

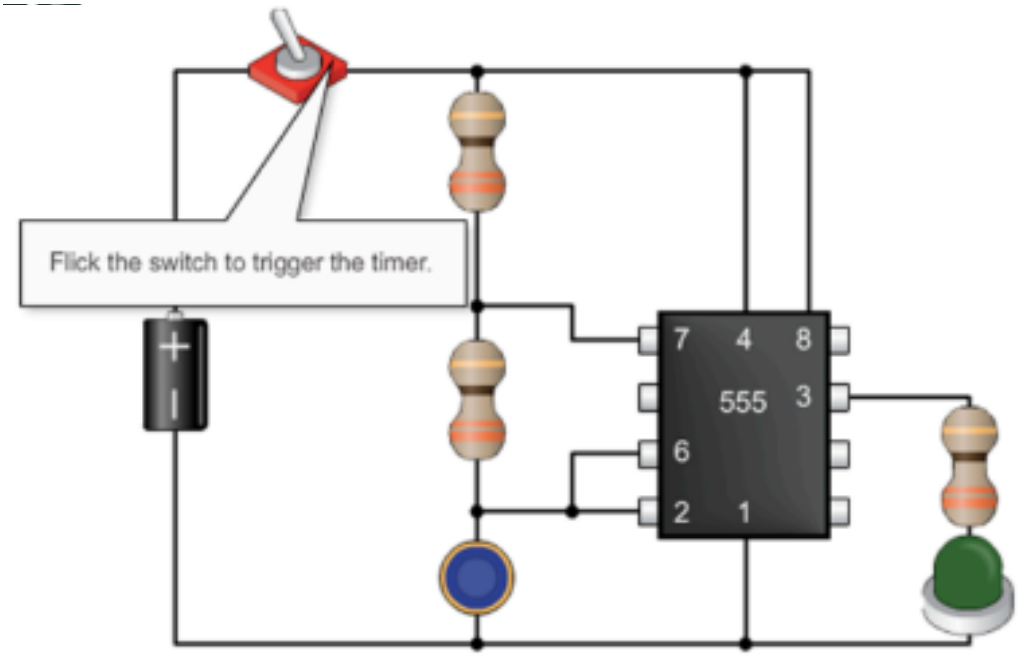
SUMMARY OPERATION TIMER IN ASTABLE MODE

- **Initial output** is at **HIGH** state.
- **T1 - OFF** state. Capacitor **C** will **start charging**.
- When voltage capacitor **C** reaches the value **2/3 VCC**, **COMP 1** will t**riggered Flip-Flop** and the **output** will **change** from **HIGH to LOW** state.
- Then, the transistor **T1** will be **ON**. Capacitor **C discharge.**
- When the voltage on the capacitor **C** reaches the value 1**/3 VCC** , **COMP 2** products **Flip-Flop will trigger** the timer **output** to be **HIGH**.
- The count will be **repeated.**



$$t_{HIGH} = 0.693\ (R_A + R_B)C$$

$$t_{LOW} = 0.693\ R_B C$$



TIMER ASTABLE MODE CIRCUIT

EQUATIONS TIMER IN ASTABLE MODE

Period, T

$$T = t_{HIGH} + t_{LOW}$$

$$t_{HIGH} = 0.693\ (R_A + R_B)C$$
$$t_{LOW} = 0.693\ R_B C$$

$$T = 0.693\ (R_A + 2R_B)C$$

Frequency, F

$$F = \frac{1}{T}$$

$$F = \frac{1}{0.693\ (R_A + 2R_B)C}$$

Duty cycle, DC

Thus, a 60% duty cycle means the signal is on 60% of the time but off 40% of the time.

$$DC = \frac{t_{HIGH}}{T} \times 100\ \%$$

$$DC = \frac{(R_A + R_B)}{(R_A + 2R_B)} \times 100\ \%$$

QUESTION FINAL ASTABLE MODE

A 555 Timer is connected as an astable multivibrator. Given the component value of stable mode, Ra= 2KΩ, Rb=4KΩ and C=0.1µF. Calculate the value of Time High (TH), Time Low (TL), Time (T), Frequency (F) and % Duty cycle (%D). Sketch output waveform at pin no.3 and pin no.6 simultaneously.

ANSWER

TH = 0.693 (Ra+Rb) C

= 0.693 (2KΩ+4KΩ) (0.1µF)

= 0.416ms

TL = 0.693 (Rb) C

= 0.693 (4KΩ) (0.1µF)

= 0.277ms

T = TH +TL

= (0.41ms+ 0.277ms)

= 0.693ms

F = 1/ T

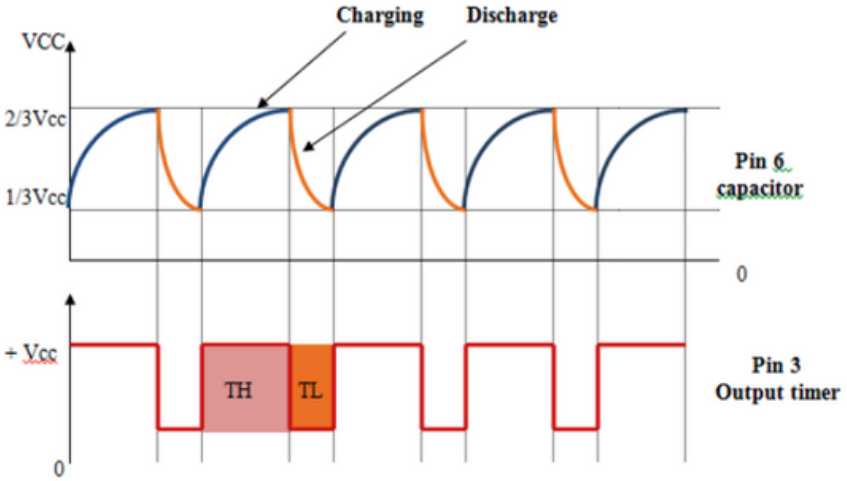
=1/0693MS

= 1449.2Hz

% Duty cycle: [TH/T) 100

= [TH/T] x 100

= 60%

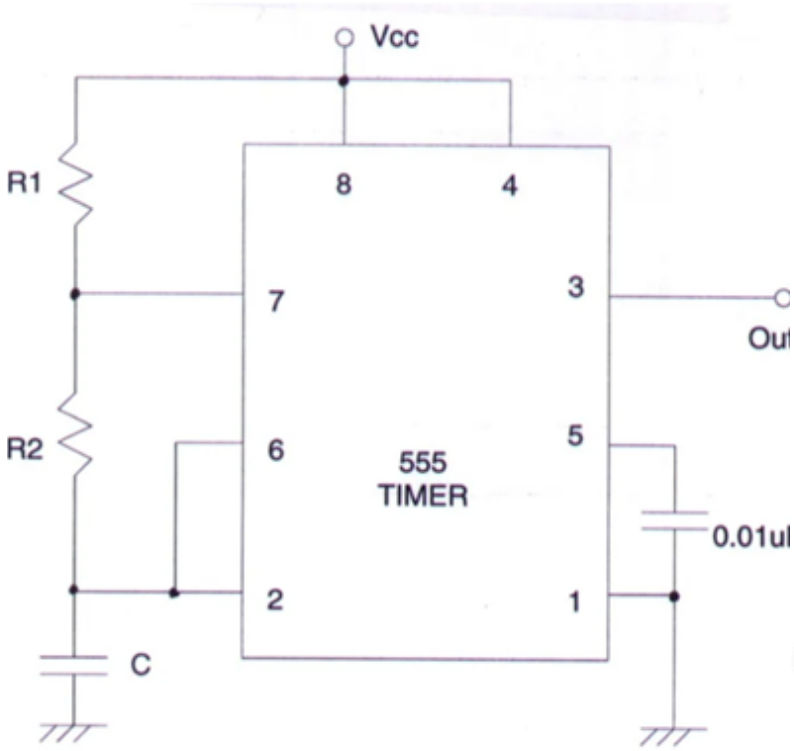


QUESTION FINAL ASTABLE MODE

Draw a 555 Astable Multivibrator completely with a frequency of 1 kHz and a mark to space ratio of 2:1. A 10nF capacitor is used in the circuit. Show all the calculations to construct the multivibrator.

ANSWER

F = 1 kHz



$$T = \frac{1}{F} = \frac{1}{1k} = 1ms$$

$$2T_H + T_L = 1ms$$

$$T_L = \frac{1m}{3} = 333.33\mu s$$

$$T_H = 2(333.33\mu) = 666.67\mu s$$

$$T_L = 0.693R_BC$$

$$333.33\mu = 0.693(R_B)(10n)$$

$$R_B = 48.1\ k\Omega$$

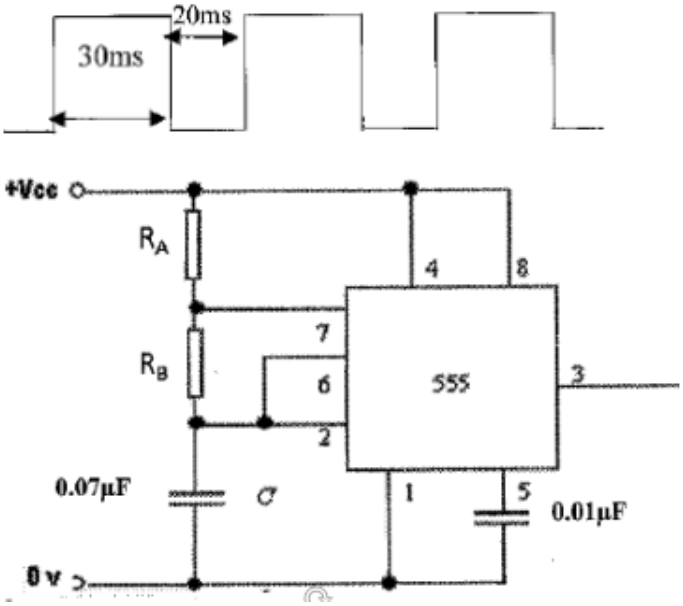
$$T_H = 0.693(R_A + R_B)C$$

$$666.67\mu = 0.693(R_A + 48.1k)(10n)$$

$$R_A = 48.1\ k\Omega$$

QUESTION FINAL ASTABLE MODE

Based on figure 1 and figure 2, calculate RA, RB, oscillation frequency (f) and % duty cycle



ANSWER

$T = T_{HIGH} + T_{LOW}$
$= 30m + 20m$
$= 50ms$

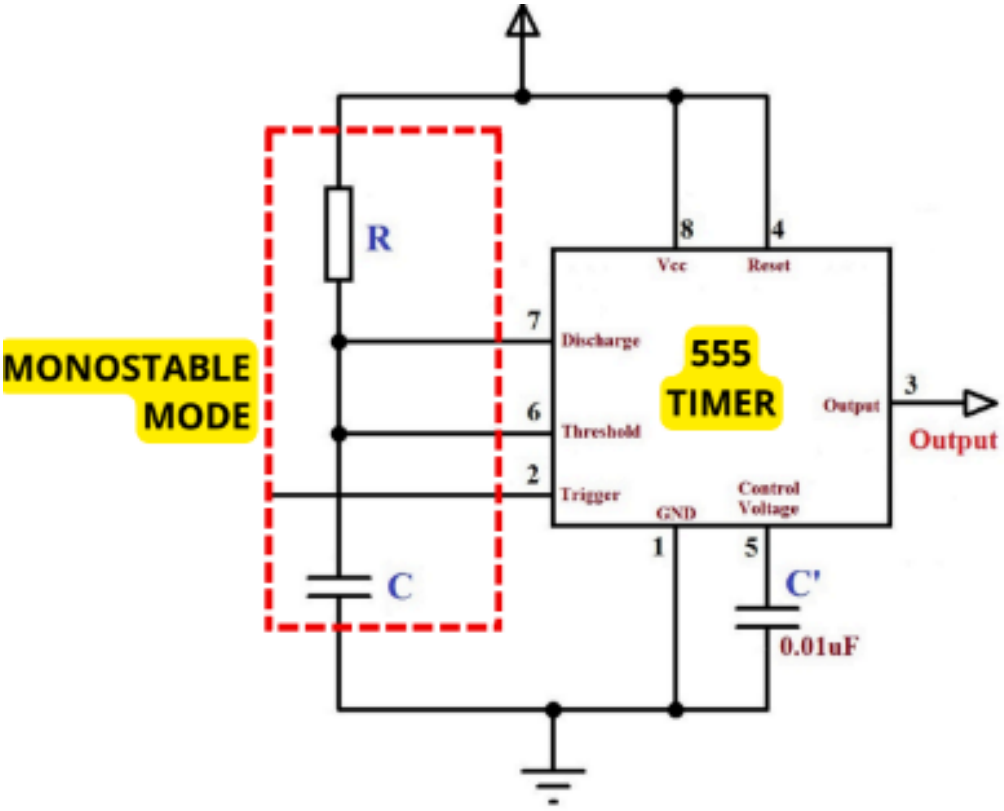
Frequency, $F = \frac{1}{T} = \frac{1}{50m} = 20\ Hz$

Duty Cycle, $\%\ D = \frac{T_{High}}{T} x\ 100\% = \frac{30m}{50m} x\ 100\% = 60\%$

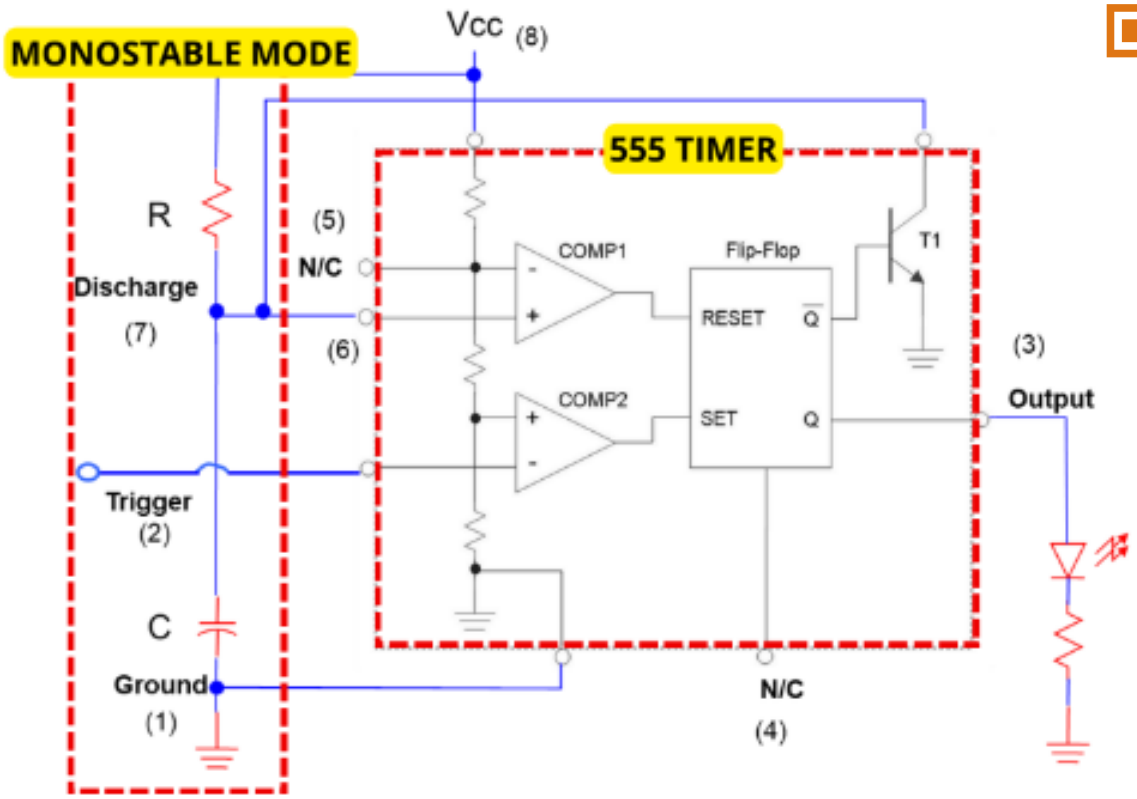
$T_{LOW} = 0.693\ R_B C$
$20m = 0.693\ R_B(0.07\mu)$
$R_B = 412.29\ k\Omega$

$T_{HIGH} = 0.693\ (R_A + R_B)\ C$
$30m = 0.693\ (R_A + 412.29)(0.07\mu)$
$R_A = 206.14\ k\ \Omega$

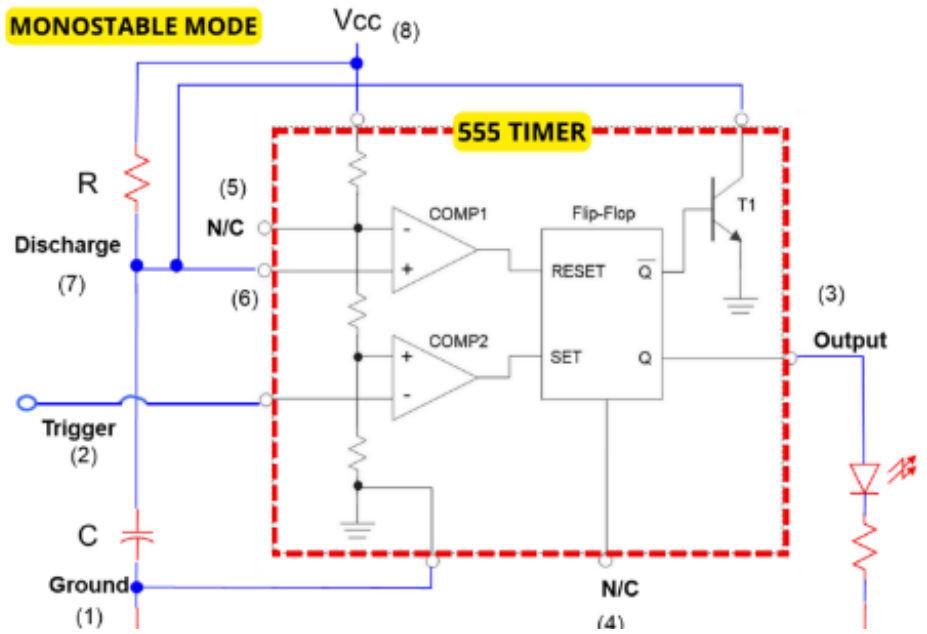
SCHEMATIC MONOSTABLE MODE



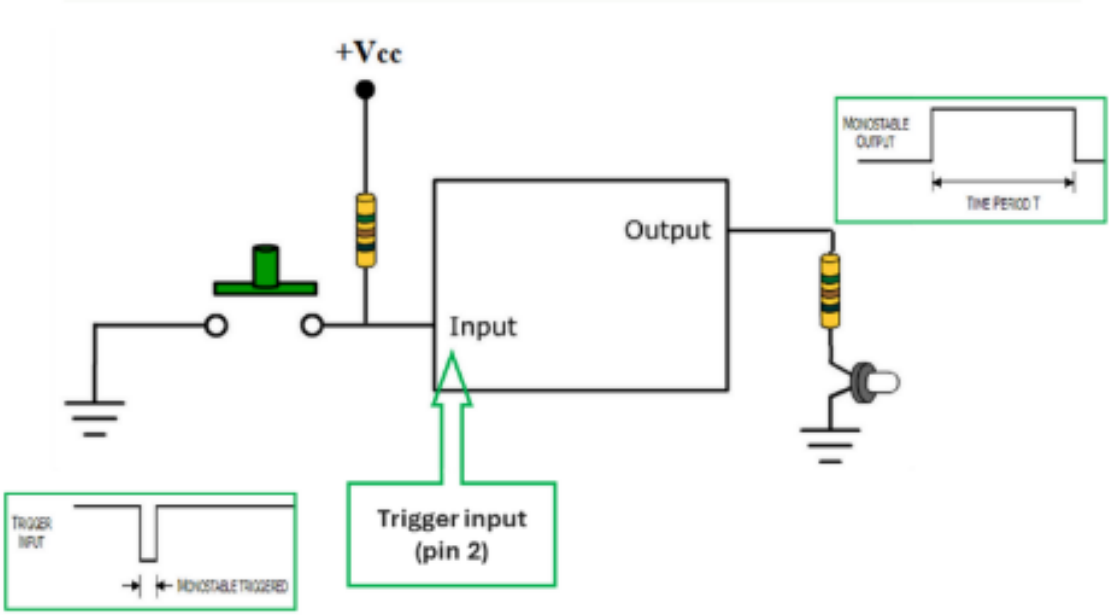
MONOSTABLE MODE



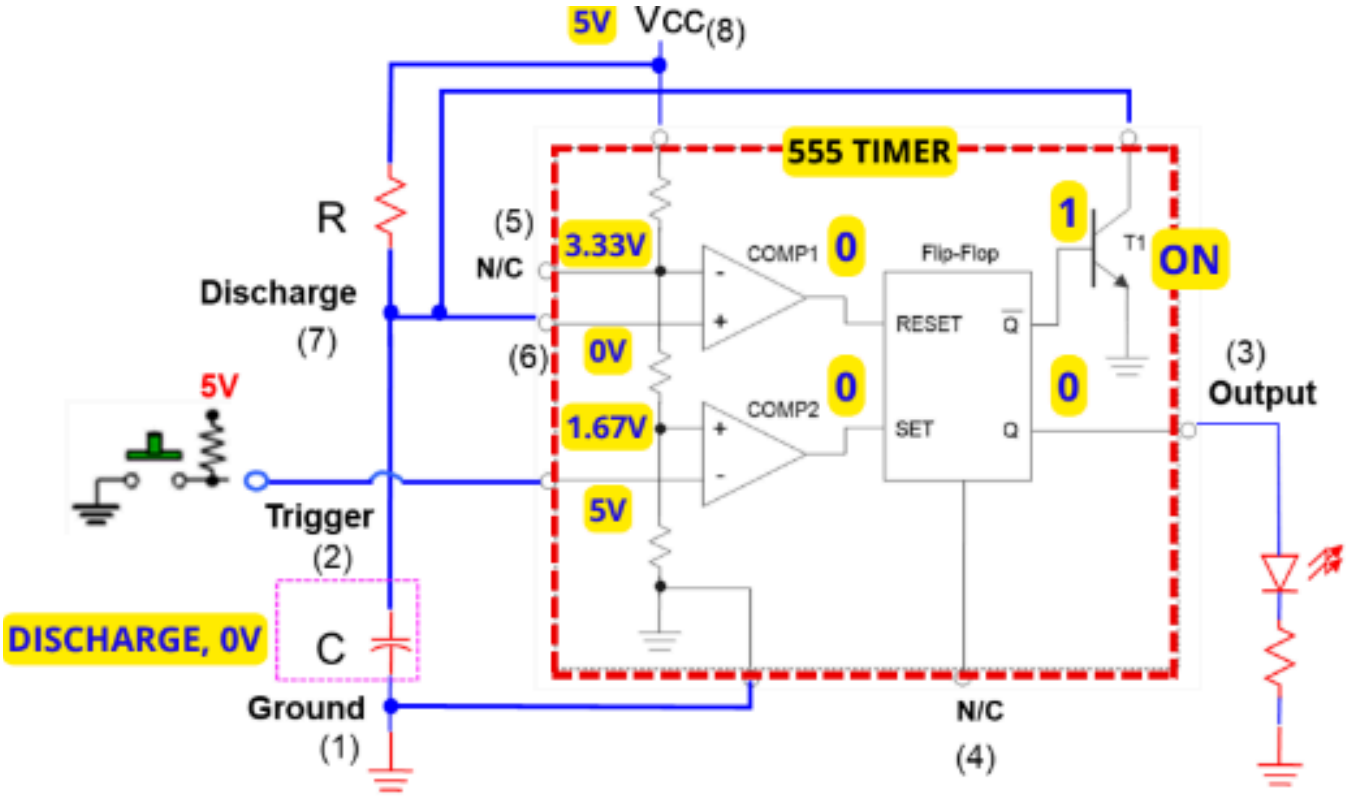
OPERATION TIMER 555 MONOSTABLE MODE



When **triggering signal** is applied to its **input,** the **output changes** from its normal **0** state **to** a logic **1** (**unstable state**) for a **certain amount of time** before it automatically **return to its stables 0 state.**



OPERATION TIMER 555 MONOSTABLE MODE

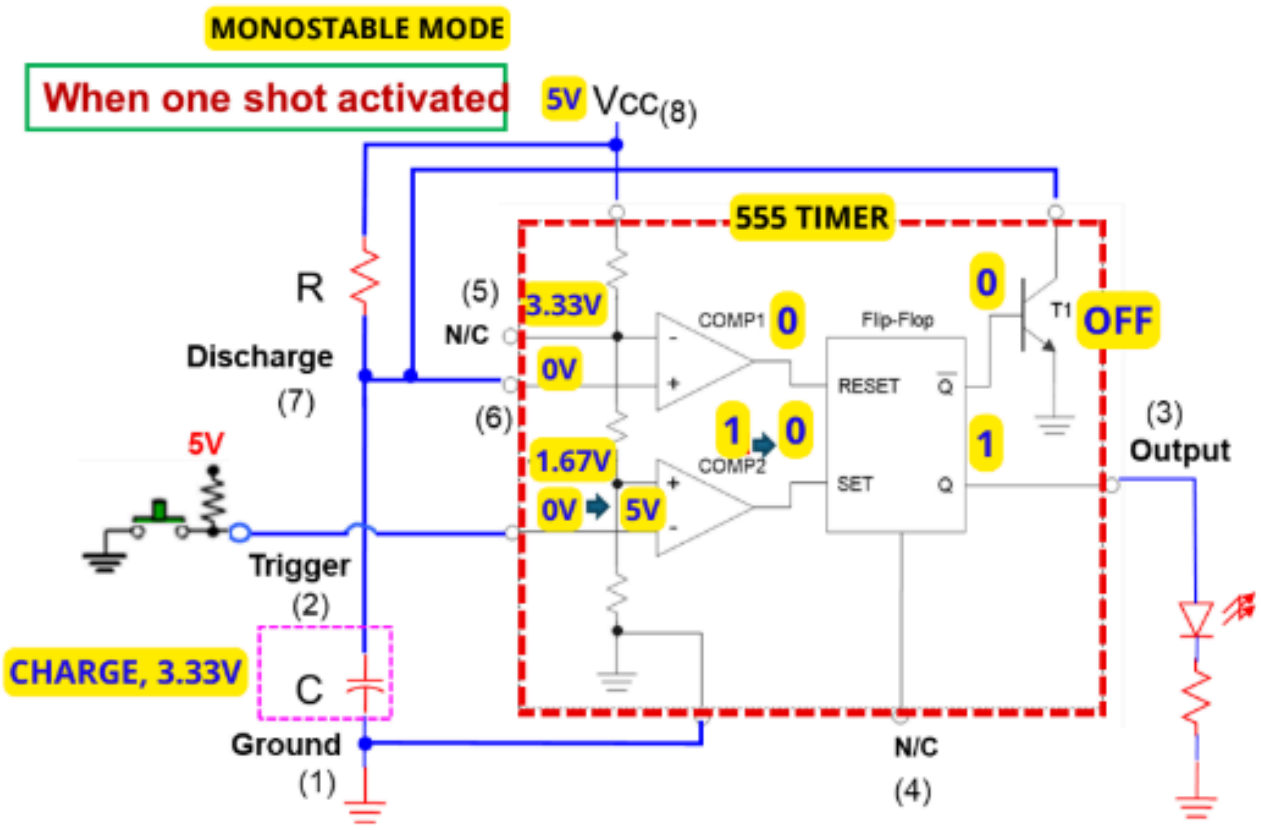


-V Comm 1: 2/3 Vcc
= 2/3(5V)
= 3.33V

+V Comm 2: 1/3 Vcc
= 1/3(5V)
= 1.67V

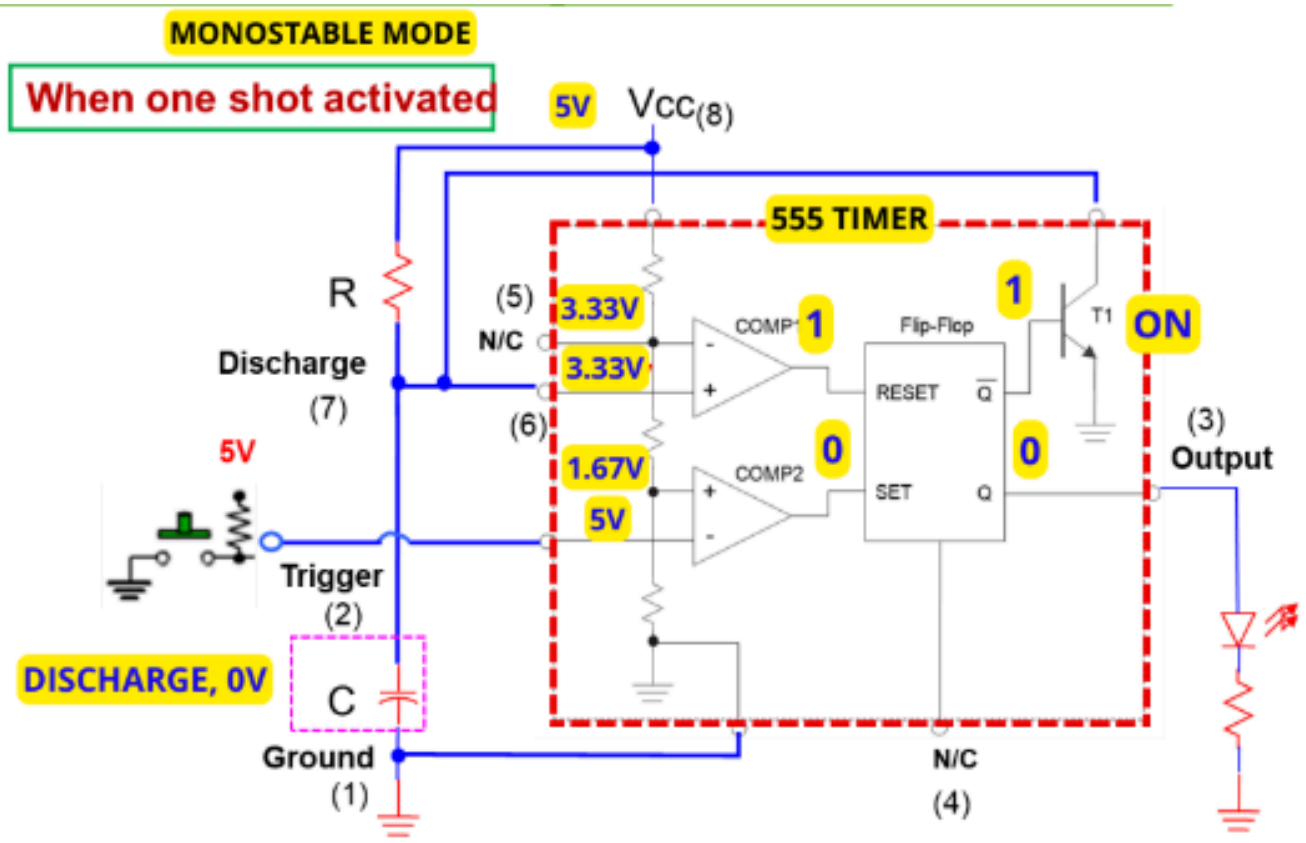
- There is **no charge** on capacitor which causes **0V** at **+ve input** of **COMP 1**. Output **COMP 1** become **0**.
- When **triggering signal is NOT applied** to its trigger input, Output **COMP 2** become **0.**
- The **output** remain **low** state.
- At this time **T1** is in **ON** state, which create a path for Capacitor **C** to **uncharged**.

OPERATION TIMER 555 MONOSTABLE MODE



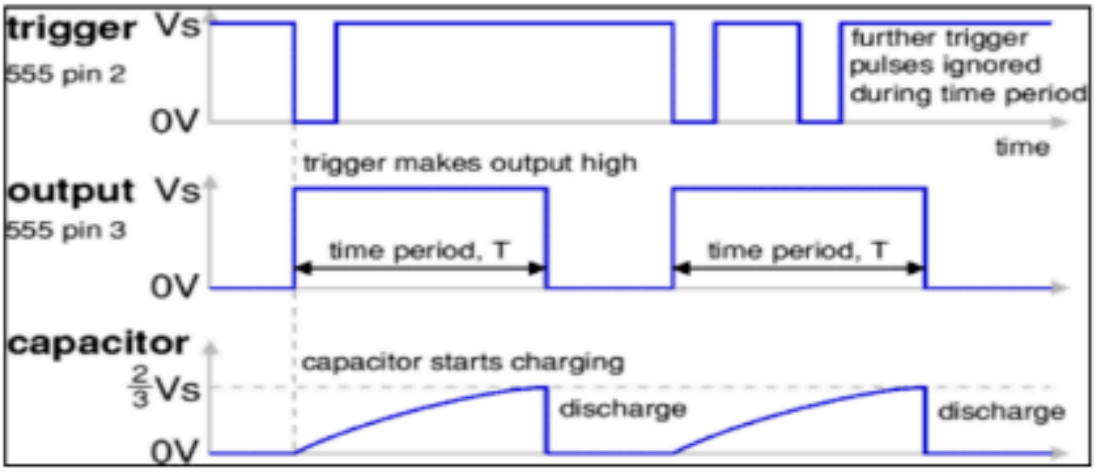
- **Capacitor** remain **uncharged**. Output **COMP 1** remain **0.**
- When the **pushbutton is close** trigger **input** goes to **0V at -ve input** of **COMP 2** because it is **shorted to Ground**. Output **COMP 2** become **1.**
- The **output** become **high** state.
- At this time **T1** is in **OFF** state, Capacitor **C begin charge**.
- When the **pushbutton is release** trigger **input goes to 5V** again at **-ve input** of **COMP 2**. Output COMP **2** change from **1** to **0**. The **output** remain **high** state.

OPERATION TIMER 555 MONOSTABLE MODE



- When **Capacitor charges to 3.33V**, Output **Comparator 1** become **1**, Output **Comparator 2** will be **0**.
- The **output** become **low** state.
- At this time **T1** is in **ON** state, provides a **discharge path to capacitor.**
- The **output** will remain in the **Low until the trigger pulse** applied to **pin 2**. This cycle will be **repeated.**

OPERATION TIMER 555 MONOSTABLE MODE



- **Before triggering** signal is applied to pin no 2 , the circuit is in stable **condition (LOW state)** and **T1 transistor ON. Capacitor C** will **bypassed ground (0V).**
- When a **negative pulse** applied to pin no 2, transistor T1 will be OFF (T1 will open circuit) will **start charging the capacitor C to + Vcc through** the resistor values of R, at this time the timer **output is HIGH**.
- **When** the voltage on the c**apacitor C reaches the value 2/3** Vcc, the output is set to the **LOW** state **causes T1** to be **ON** and **capacitor discharge.**
- The **output** will remain in the **LOW until the trigger pulse applied to pin 2**. This **cycle will be repeated**.
- A **monostable circuit produces a single output** pulse when **triggered.**
- It is called a monostable because it i**s stable in just one state**: **'output low'.**
- The **'output high' state is temporary.**
- The **duration of the pulse** is called the **time period (T) /pulse width(W)** and this is determined by resistor R and capacitor C.

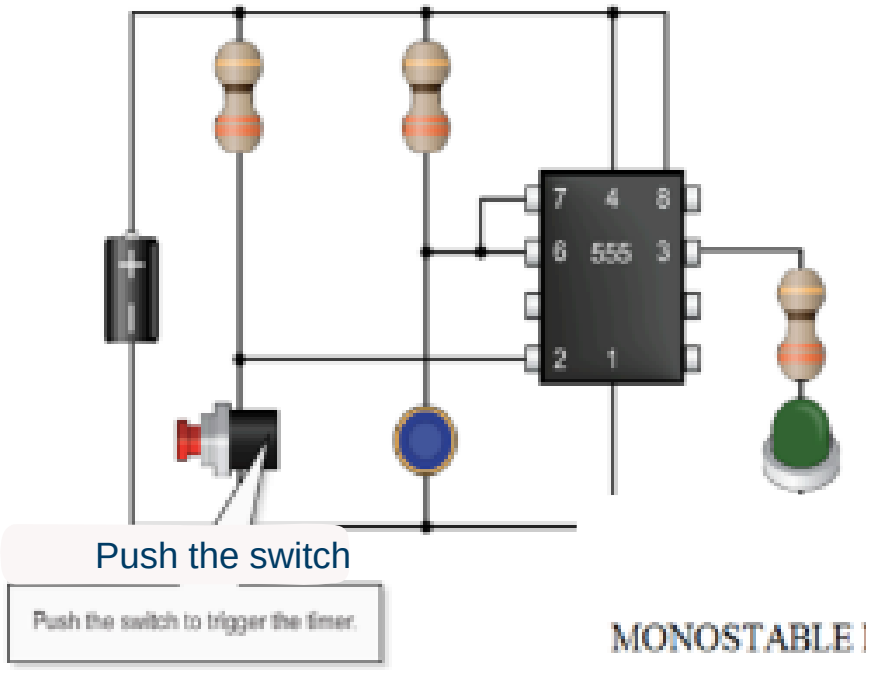
W (pulse width) = 1.1 RC *seconds*

R = resistance in ohms
C = capacitance in farads (F)

Time period (T) / Width(w) = Time period in seconds (s)

Maximum reliable time period is about 10 minutes.

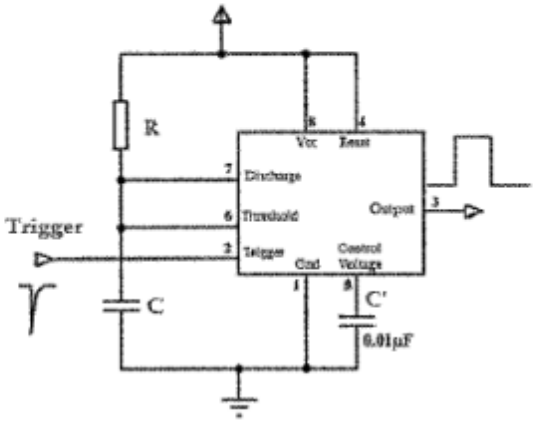
SIMPLE APPLICATION OF TIMER MONOSTABLE MODE



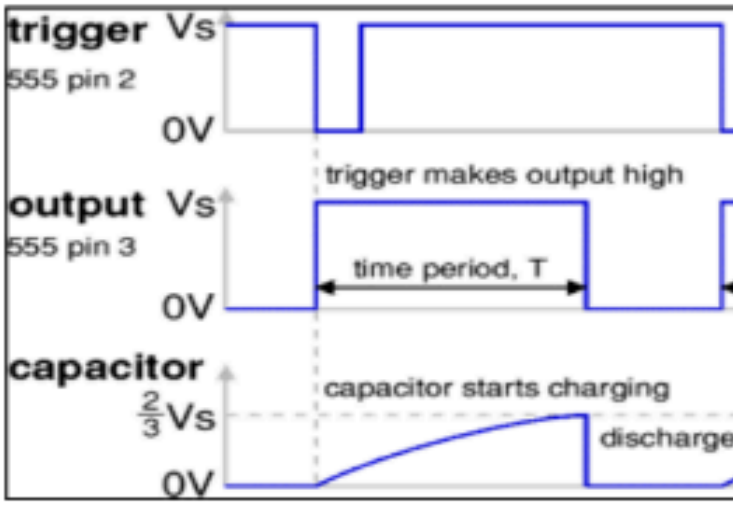
- In this circuit, the 555 timer is set to turn on the LED when the push switch is pressed; the led will be light for a certain amount of time .
- This is a monostable circuit as it works only once.
- The switch must be pressed again for the led to light again.
- the length of the time period - ie how long the output is on for - is determined by a resistor/capacitor network (RC network), which is connected to pins 6 and 7.
- The RC network is a combination of resistors and capacitors used to control this time period.
- The resistor 'slows-down' the current, which charges the capacitor.

QUESTION FINAL MONOSTABLE MODE

By referring to below figure, sketch the waveform at pin 2, pin 3 and pin 6. Then, calculate the pulse width if R = 10 kΩ and C = 0.1nF.



ANSWER

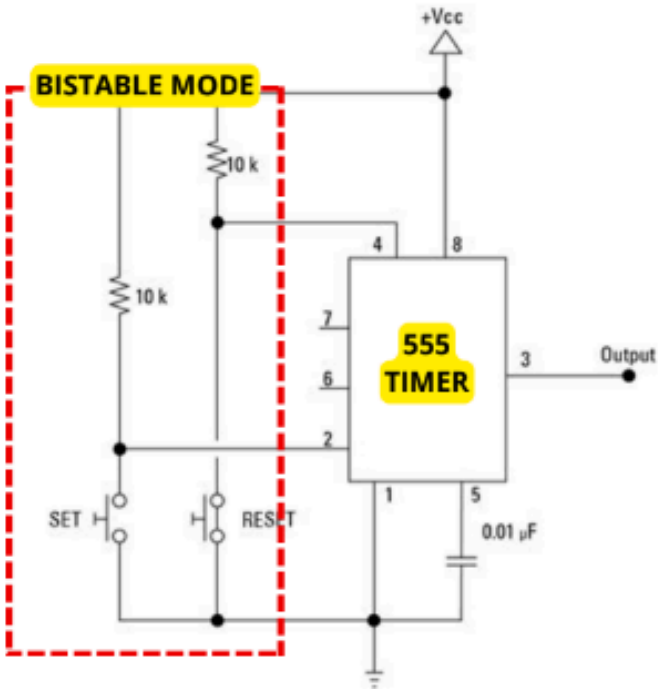


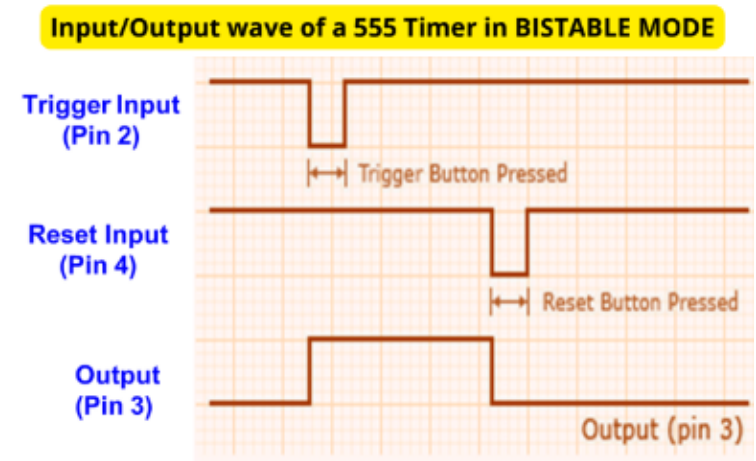
$$T = 1.1\ RC$$

$$= 1.1 \times 10k \times 0.1n$$

$$= 1.1\ \mu s$$

OPERATION TIMER 555 BISTABLE MODE





When **triggering** signal is **applied to its input,** the **output changes** from its normal **0** state to a logic **1** (unstable state) for a **certain amount of time before it automatically return to its stables 0 state.**

- Bistable circuits are known a bistable because it is **stable in two states: output high and output low.**

- It is also known **as a 'flip- flop':** flip to one state when **triggered**, then **flop** back
- to the other state when **reset** no timing involved

- Bistable circuits can be **used in switching and latching circuits, counters, shift registers, and primitive memory circuits.**

- They can also be used in **relay control circuits.**

- It has **two inputs:**
  Trigger (555 pin 2) makes the **output high.**
  Trigger is 'active low' , it functions when < 1/3 Vcc.

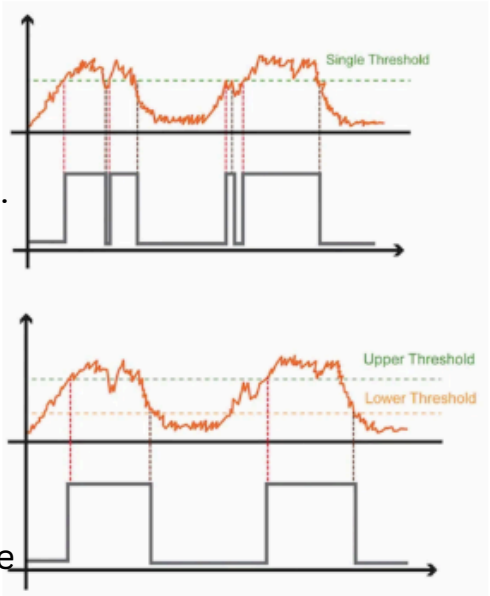
  Reset (555 pin 4) makes the **output low.**
  Reset is 'active low',, it resets when < 2/3 Vcc.

BISTABLE MODE

- Taking the **Trigger input low** makes the **output** of the circuit go into the **high state**.
- Taking the **Reset input low** makes the **output** of the circuit go into the **low state.**

OPERATION TIMER 555 SCHMITT TRIGGER

- Schmitt Trigger is a special type of comparator that is **used to avoid not clean (noisy) signals**.



- A **comparator** is a device that c**ompares two voltages and** t**he outcome is the indication** of whether one voltage is higher than the other or not.
- Schmitt trigger, also called as **Regenerative Comparator,** compares the input voltage to two reference voltages and produces an equivalent output.
- The **output** of a Schmitt trigger is **always a square** or **rectangular wave** irrespective of the shape of the input.

- It is often used when we need to do the following:

1. **Convert sine wave to square wave**
2. **To clean up the noisy signals**
3. **To convert slow edges (like in a triangular wave) into fast edges (like a square wave)**

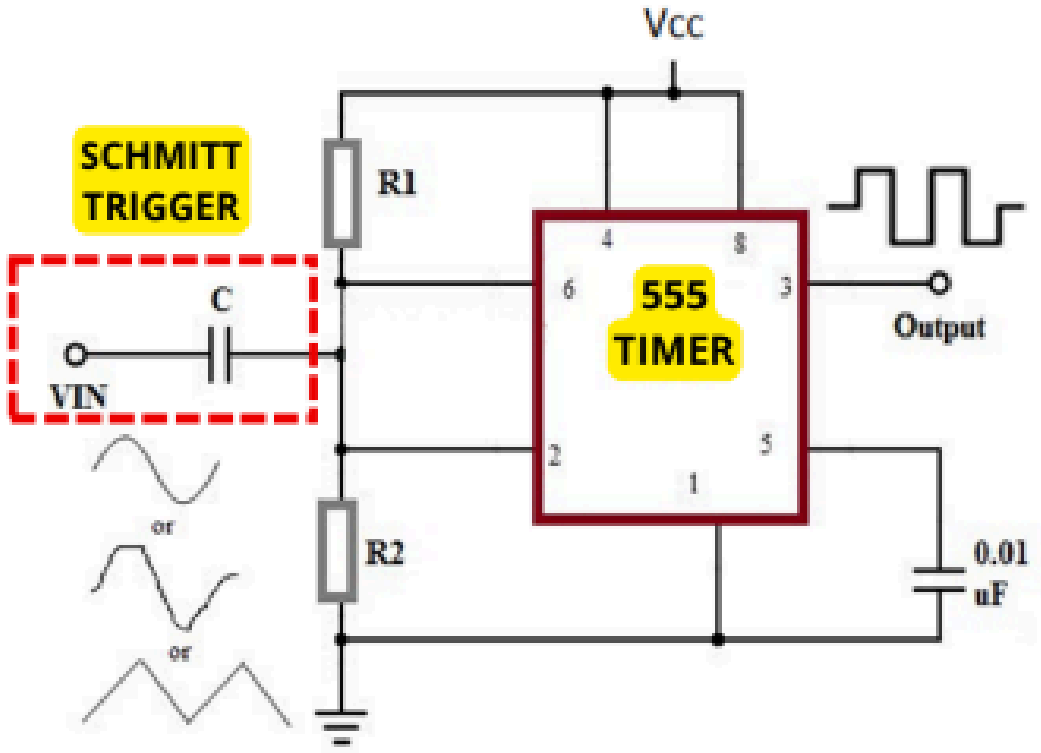
Schmitt can be constructed from a 555 timer.

A Schmitt trigger is a circuit which **generates an output waveform of a square wave.**

implemented on several devices - most commonly **on the operational amplifier.** Schmitt triggers are commonly **used in signal conditioning applications to remove noise in digital circuits.**

The Schmitt trigger's **primary function is to remove noise** in waveforms to **prevent fluctuations** from causing unpredictable output changes.

OPERATION TIMER 555 SCHMITT TRIGGER

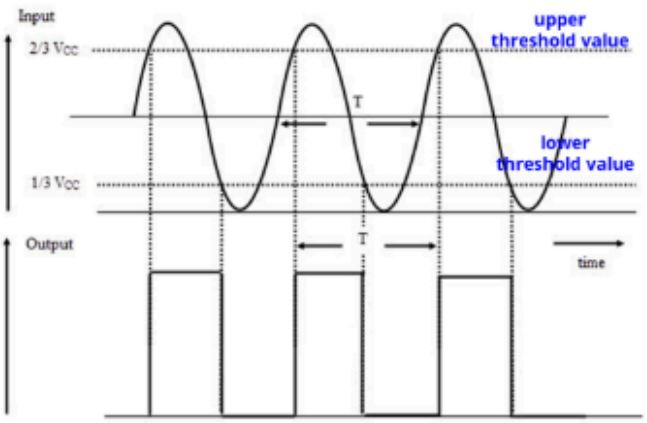


- Pins **4 and 8** are connected to the supply (**VCC**).
- The pins **2 and 6** are tied together and the **input** is given to this common point through a capacitor C.
- This common point is supplied with an external bias voltage of **VCC / 2** with the help of the **voltage divider** circuit formed by the resistors **R1 and R2.**

TRIGGER MODE

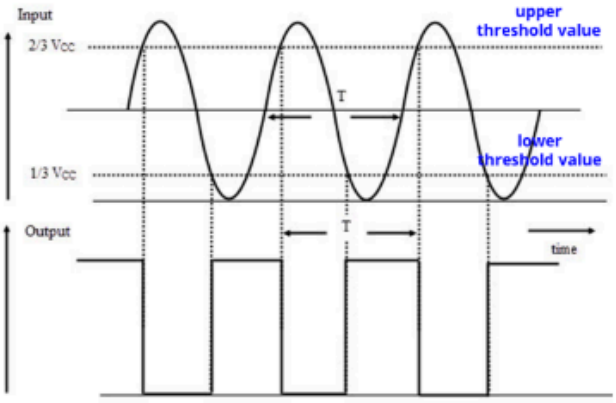
OPERATION TIMER 555 SCHMITT TRIGGER

NonInverting Schmitt Tigger



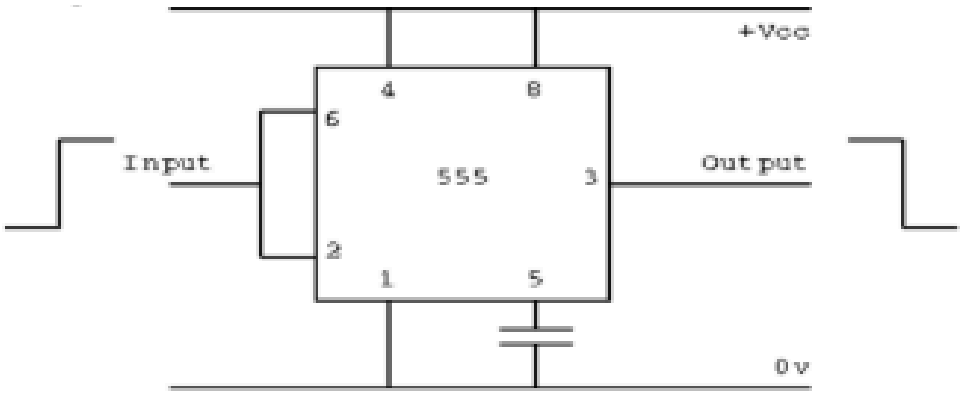
- The important **characteristic** of the **Schmitt trigger is Hysteresis.**
- The **output** of the Schmitt trigger **is high if** the input **voltage is greater than the upper threshold value.**
- The **output** of the Schmitt trigger **is low if** the **input voltage is lower than the lower threshold value.**
- **Input high (> 2/3 Vcc) makes output high, +Vcc.**
- **Input low (< 1/3 Vcc) makes output low, 0V**
- When the **input voltage** is **between 1/3 and 2/3 Vcc** the **output** remains in its **present state**.
- This intermediate **input region** is a **deadspace** where there is **no response**, a property **called hysteresis**, it is like backlash in a mechanical linkage.

Inverting Schmitt Tigger



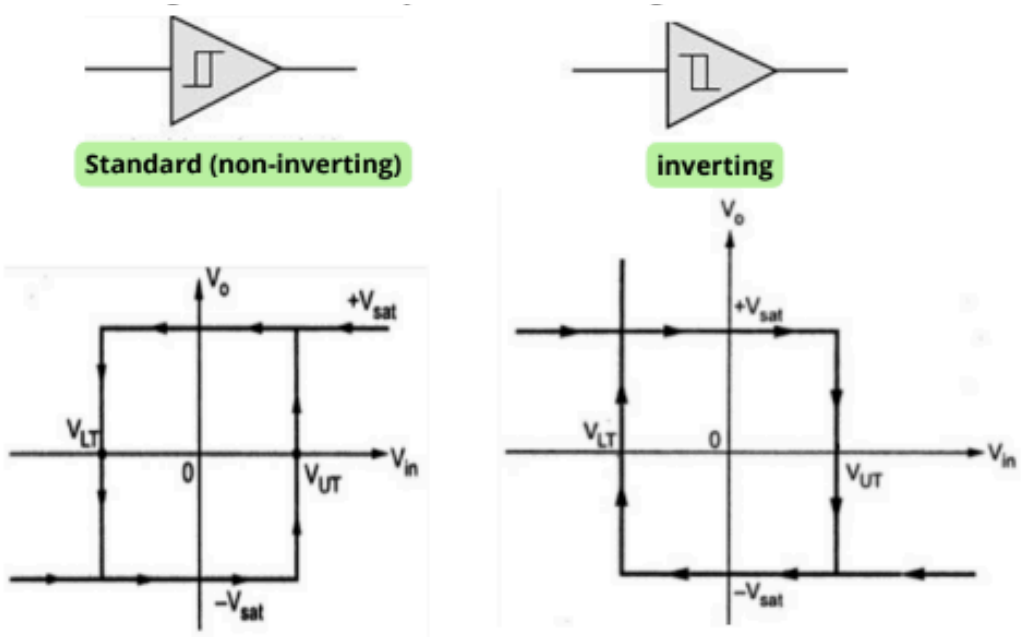
- It is an i**nverting buffer or NOT gate** because the output logic state
- (low/high) is the inverse of the input state:
- **Input low (< 1/3 Vcc) makes output high, +Vcc**
- **Input high (> 2/3 Vcc) makes output low, 0V**
- When the input voltage is between 1/3 and 2/3 Vs the output remains in its present state.

OPERATION TIMER 555 SCHMITT TRIGGER A BUFFER



- A **buffer** circuit **allows an input circuit** to be **connected to an output circuit,** it is like an interface between one circuit and another.
- The buffer circuit's **input has a very high impedance** (about 1M) so it requires only a **few µA**, but the output can sink or source up to 200mA.
- This **enables a high impedance** signal source (such as an LDR) to **switch a low impedance output transducer** (such as a lamp).
- The circuit **acts like an inverter or NOT gate.**
- When the **input is held low,** the **output is high** and will **provide (source) current.**
- When the **input is held high**, the **output is low** and will **sink current.**
- For a buffer for even higher power devices that requir currents, the **555 buffer can be used to drive a transistor circuit**

SYMBOLS SCHMITT TRIGGER



Transfer characteristics

- There are basically **two symbols for the Schmitt Trigger.**
- The symbol is a triangle with an input and an output.
- Inside there is the hysteresis symbol.
- **Depend**ing on the type of Schmitt Trigger, **inverting or non- inverting (standard), the hysteresis curve sign differs.**

APPLICATION SCHMITT TRIGGER

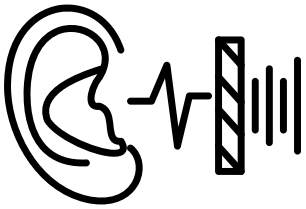
- Schmitt triggers are **mostly used to convert a sine wave into a square wave.**
- They are useful in **switch de-bouncer circuits to clean up or speed up slow or noisy input signals.**
- These triggers are often **used in signal conditioning to remove noise from signals** in digital circuits.
- Additionally, they can work as simple **ON/OFF controllers**.
- For example, They can also act as simple ON / OFF Controllers (for example, temperature based switches or it could be used with a thermistor for heating control, or with an LDR for light control circuits.

FILTERS

SCAN HERE

FILTERS

WHAT IS A FILTER?



FILTER CIRCUIT

Noise stereo system

Best sound quality

- A circuit capable of selectively filtering one frequency or range of frequencies out of a mix of different frequencies in a circuit.
- A common need for filter circuits is in high-performance stereo systems, where certain ranges of audio frequencies need to be amplified or suppressed for best sound quality and power efficiency.

FILTER APPLICATION

SPEAKERS & FREQUENCY ROUTING

Filters direct high frequencies to tweeters and low frequencies to woofers.

EQUALIZERS (EQS)

EQs use filter circuits to boost or cut specific frequencies, letting users tailor audio to suit environments

NOISE REDUCTION

Filters target and remove unwanted background hiss, hum, or static.

TELECOMMUNICATIONS

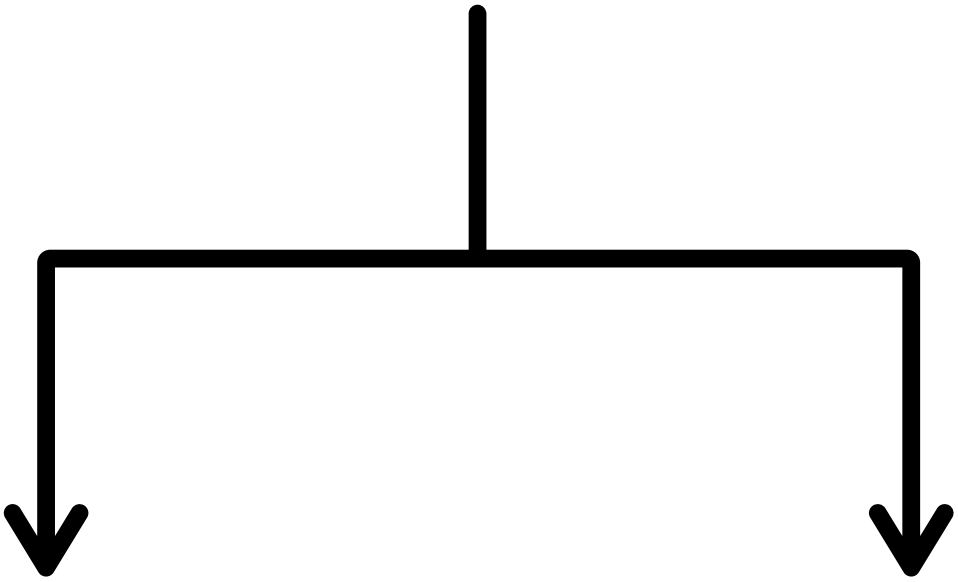
Signal transmission:
Filters clean up signals by removing noise, so communication stays clear.
Data transmission:
Digital filters in devices like modems reduce noise and help process data accurately.

POWER SUPPLIES

Smoothing:
Low-pass filters remove the AC ripple from rectified DC power, providing a smoother, more stable voltage.
Noise reduction:
Filters remove unwanted high-frequency noise from power lines, preventing interference with sensitive electronic equipment

TYPES OF FILTER

TYPES OF FILTER



PASSIVE FILTER

A passive filter is an electronic circuit made using only passive components such as resistors (R), capacitors (C), and inductors (L) that is used to filter specific frequencies from a signal.

ACTIVE FILTER

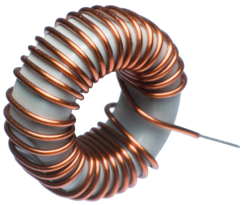
An active filter is an electronic circuit that uses active components such as operational amplifiers (op-amps), along with resistors and capacitors.

PASSIVE FILTER

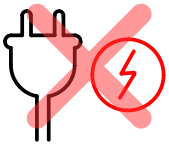
- Passive filters are based on combinations of resistors (R), inductors (L), and capacitors (C).


CAPACITOR


RESISTOR


INDUCTOR

- Passive filters <u>do not require a power</u> supply.

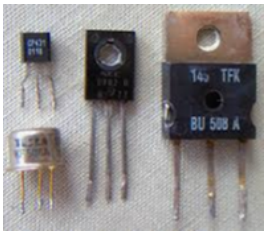


TYPES OF PASSIVE FILTER

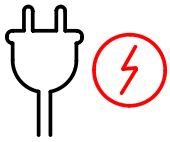
- LOW-PASS FILTER
- HIGH-PASS FILTER
- BAND-PASS FILTER

ACTIVE FILTER

- Active filters contain active components such as operational amplifiers, transistors, or FETs within their circuit design.



- Active filters <u>need power</u> from an external source and use it to boost or amplify the output signal.



TYPES OF ACTIVE FILTER

LOW-PASS FILTER

HIGH-PASS FILTER

BAND-PASS FILTER

DIFFERENCES BETWEEN PASSIVE FILTER AND ACTIVE FILTER

Passive Filter	Active Filter
Use passive component such as resistors, capacitors and inductors.	Contain active components such as operational amplifiers, transistors, or FETs within their circuit
An external power source is not required.	Need power from an external source.
Low voltage gain.	High voltage gain.
It uses a simple circuit.	Its circuitry is complex.
Suitable for high frequency.	Suitable for low frequency.
Has no frequency limitations.	Has frequency limitation due to limited bandwidth of op-amp.

CUT OFF FREQUENCY, FC

Definition:

- This "Cut-off", "Corner" or "Breakpoint" frequency is defined as being the frequency point where the capacitive reactance and resistance are equal, R = Xc
- When this occurs the output signal is attenuated to **70.7%** of the **input signal value** or **-3dB [20 log(Vout/Vin)] of the input.**

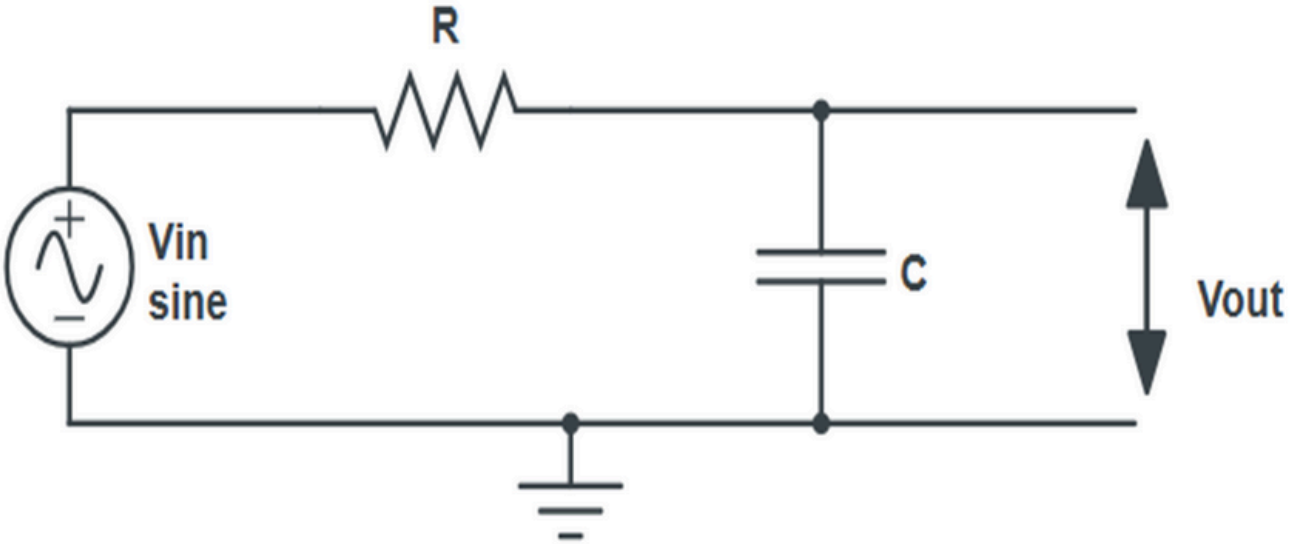
Voltage gain in dB = 20 log 10 0.707 = - 3dB

- **Formula for fc :** $f_c = \frac{1}{2\pi RC} Hz$

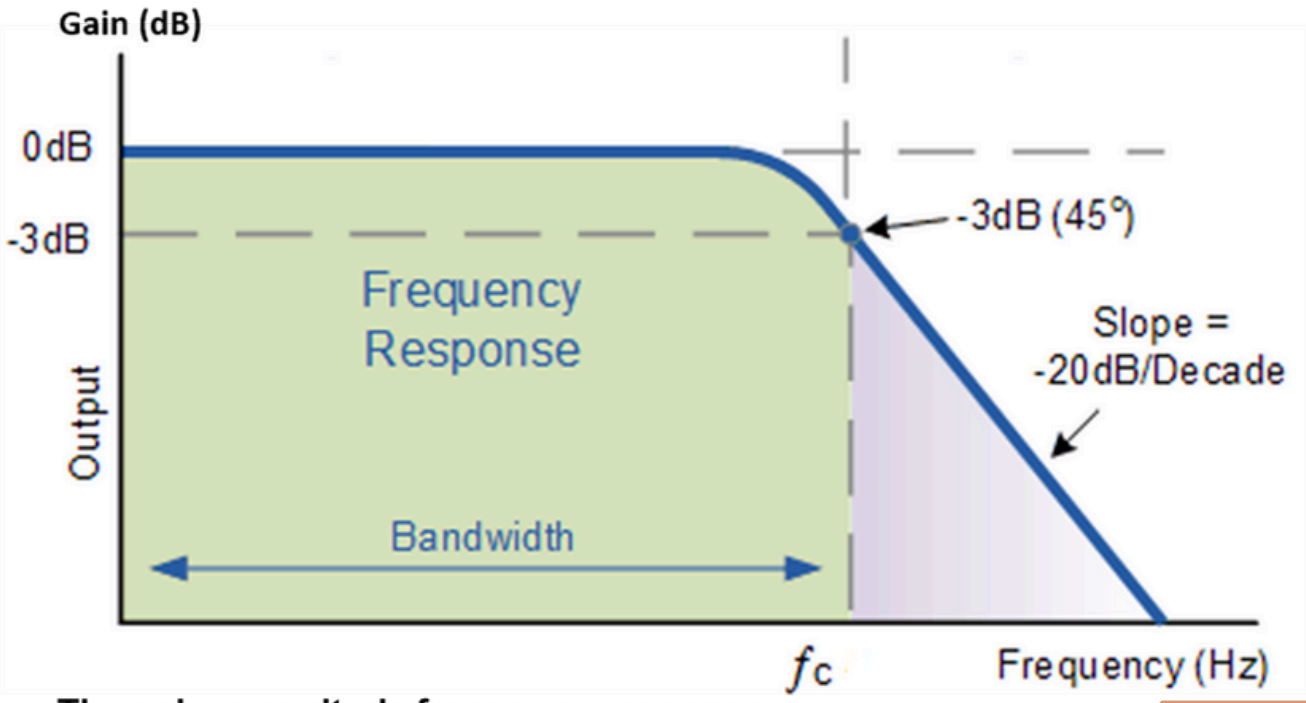
PASSIVE LOW PASS FILTER

DEFINITION OF LOW PASS FILTER:

A low-pass filter allows frequencies below its cutoff frequency (fc) to pass through and attenuates frequencies above the cutoff frequency (fc).



LOW PASS FILTER CIRCUIT



The gain-magnitude frequency response

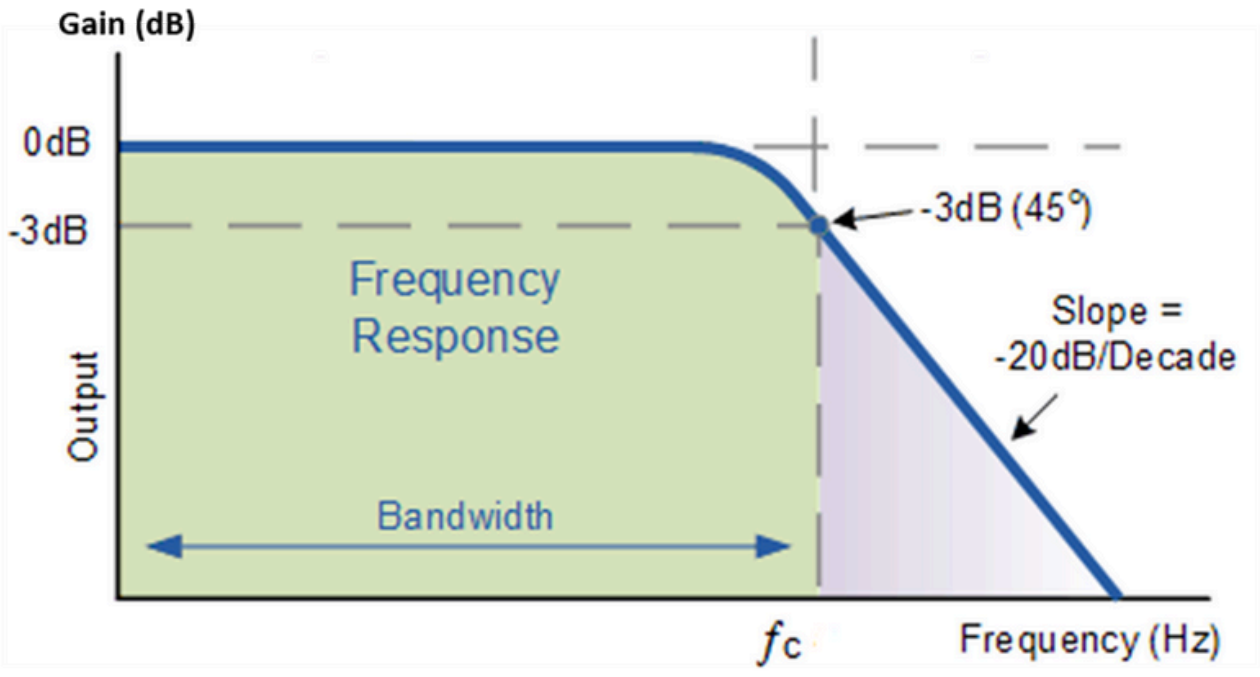
PASSIVE LOW PASS FILTER

LOW PASS CUT OFF FREQUENCY, fc:

The cutoff frequency of a low-pass filter is the frequency at which the output (load) voltage equals 70.7% of the input (source) voltage. Above the cutoff frequency, the output voltage drops below 70.7% of the input. Below the cutoff frequency, the output remains higher than 70.7%.

Phase shift angle is -45

$$f_{cutoff} = \frac{1}{2\pi RC}$$

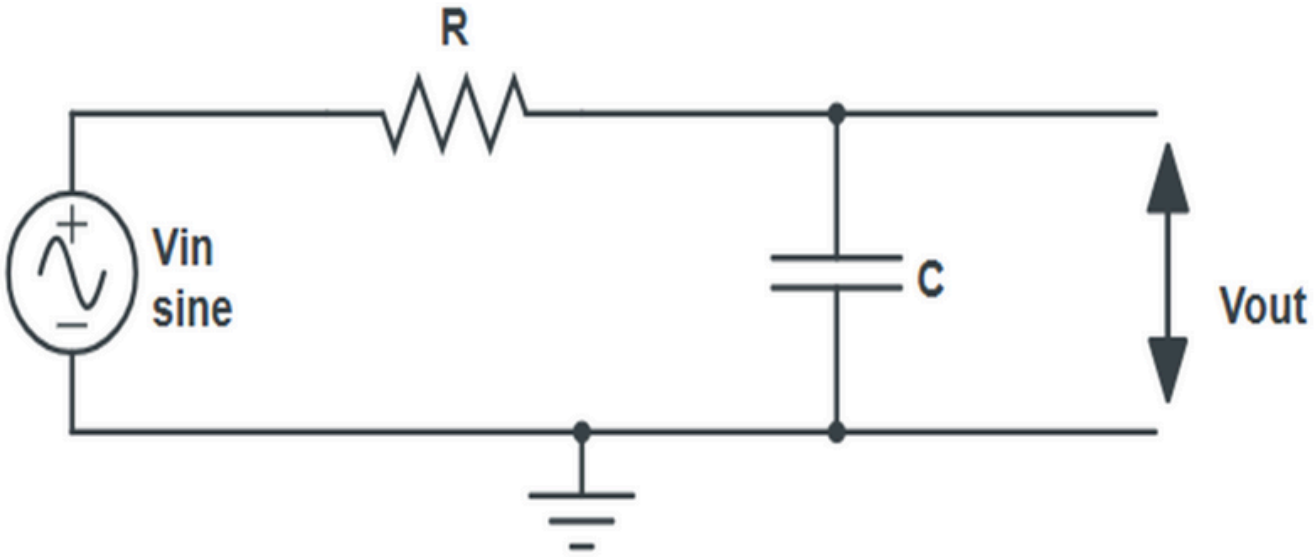


The gain-magnitude frequency response

PASSIVE LOW PASS FILTER

BASIC CIRCUIT OF LOW PASS FILTER:

Also known as **First -order Low Pass Filter**.

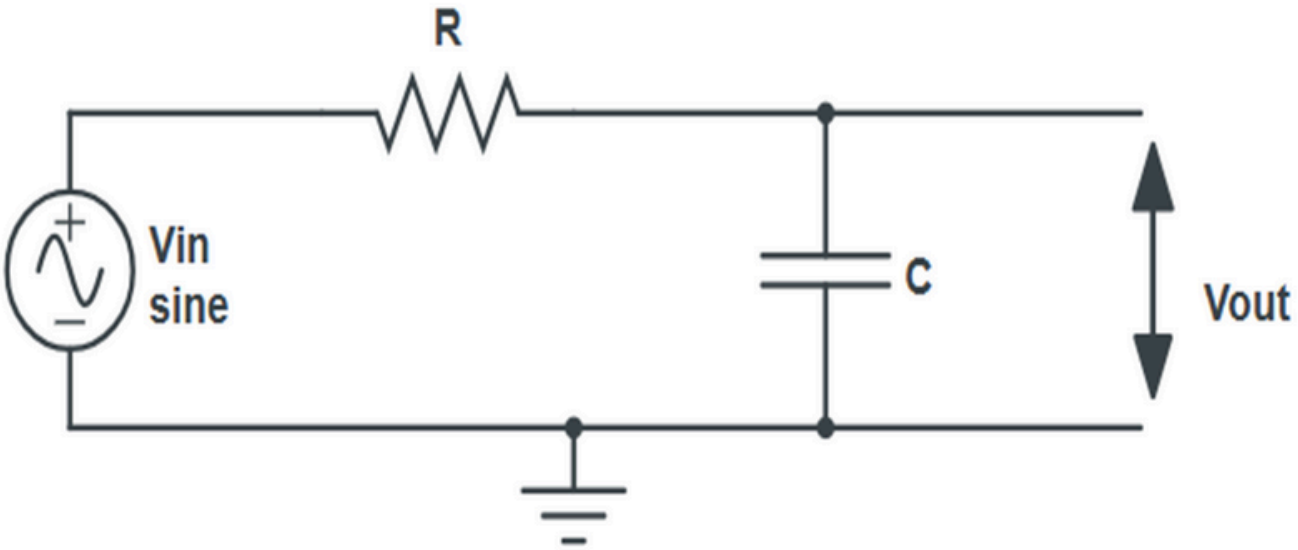


$$f_c = \frac{1}{2\pi RC}$$

$$A_V = \frac{V_{output}}{V_{input}}$$

$$A_{V(dB)} = 20 \log A_V$$

PASSIVE LOW PASS FILTER



$$V_{out} = V_{in} \times \frac{X_C}{\sqrt{R^2 + X_C^2}} = V_{in} \frac{X_C}{Z}$$

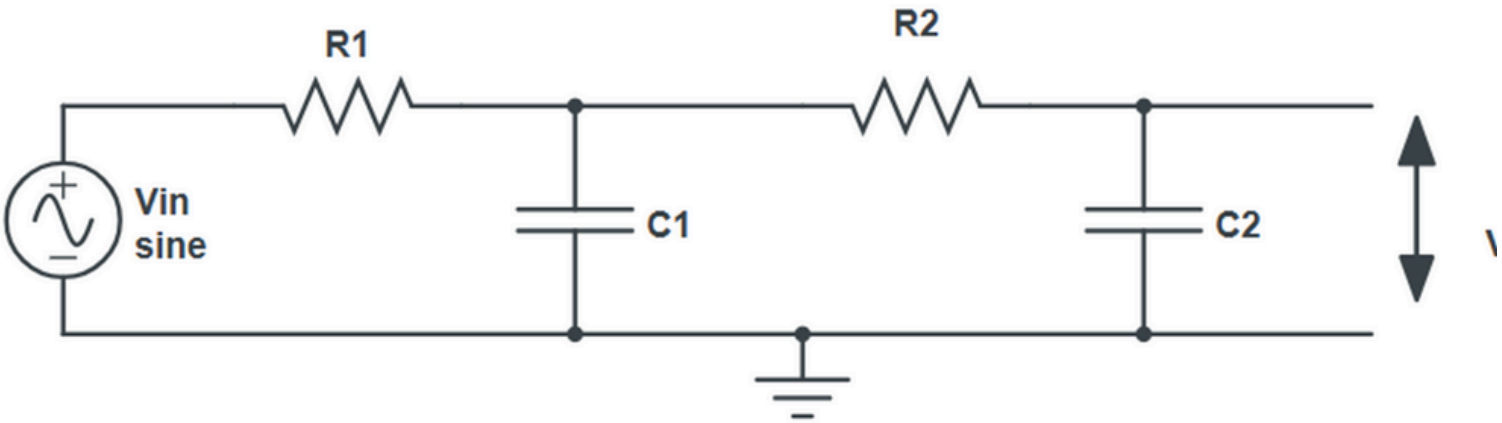
$$X_C = \frac{1}{2\pi f C} \text{ in Ohm's}$$

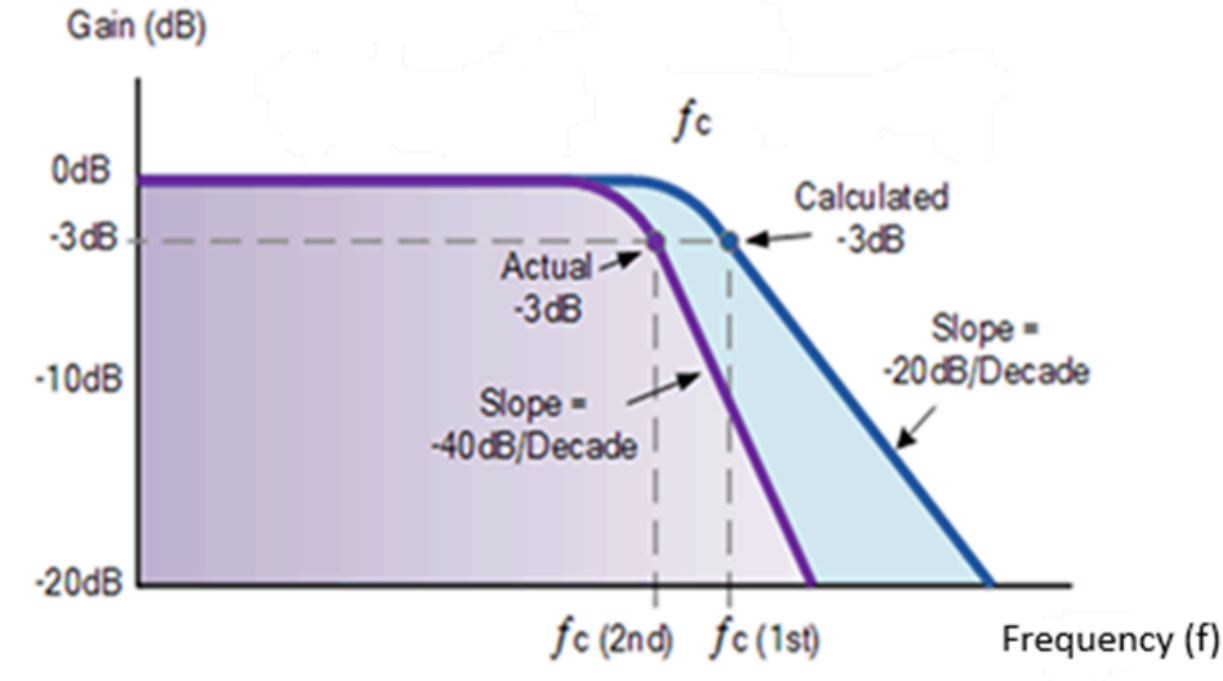
$$Z = \sqrt{R^2 + X_C^2}$$

PASSIVE LOW PASS FILTER

CASCADED LOW PASS FILTER CIRCUIT:

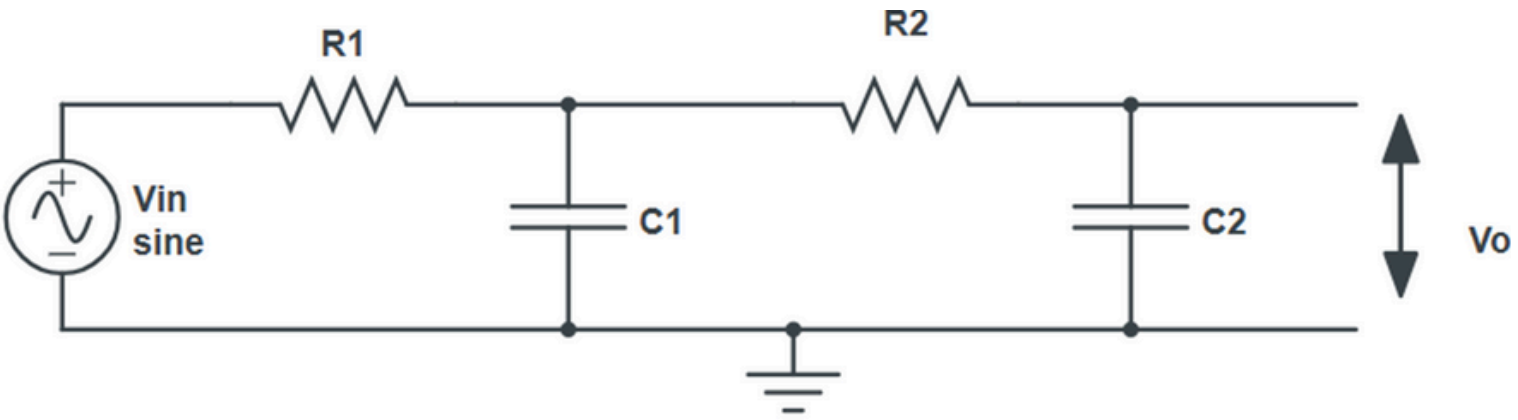
Also known as **second-order low pass filter**.





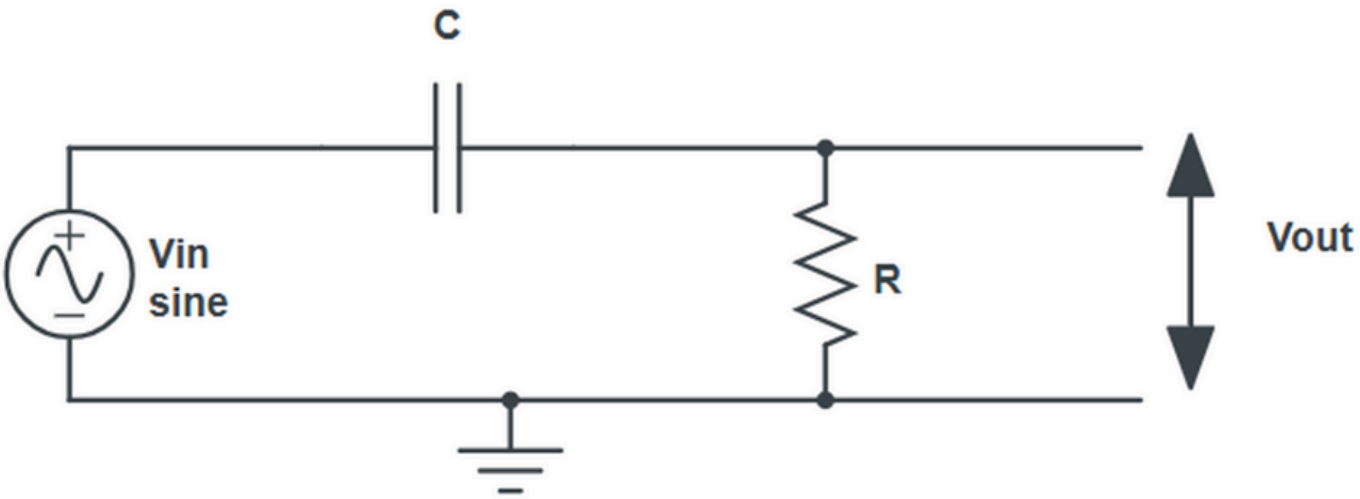
The gain-magnitude frequency response

PASSIVE LOW PASS FILTER



$$f_C = \frac{1}{2\pi\sqrt{R_1 C_1 R_2 C_2}} \text{ Hz}$$

PASSIVE HIGH PASS FILTER

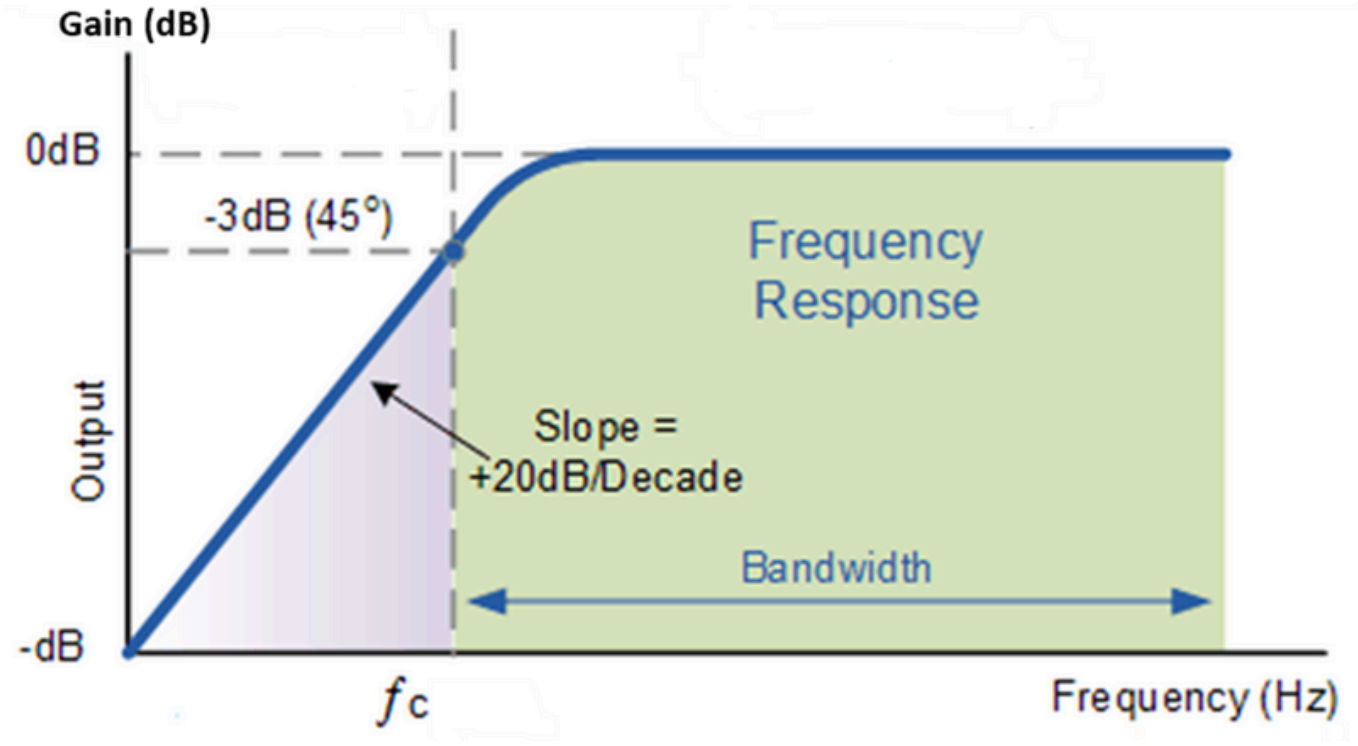


HIGH PASS FILTER CIRCUIT

PASSIVE HIGH PASS FILTER

1.DEFINITION OF HIGH PASS FILTER:

A high-pass filter allows signals with frequencies above the cutoff frequency (fc) to pass through, while attenuating signals with frequencies below cutoff frequency (fc).



The gain-magnitude frequency response

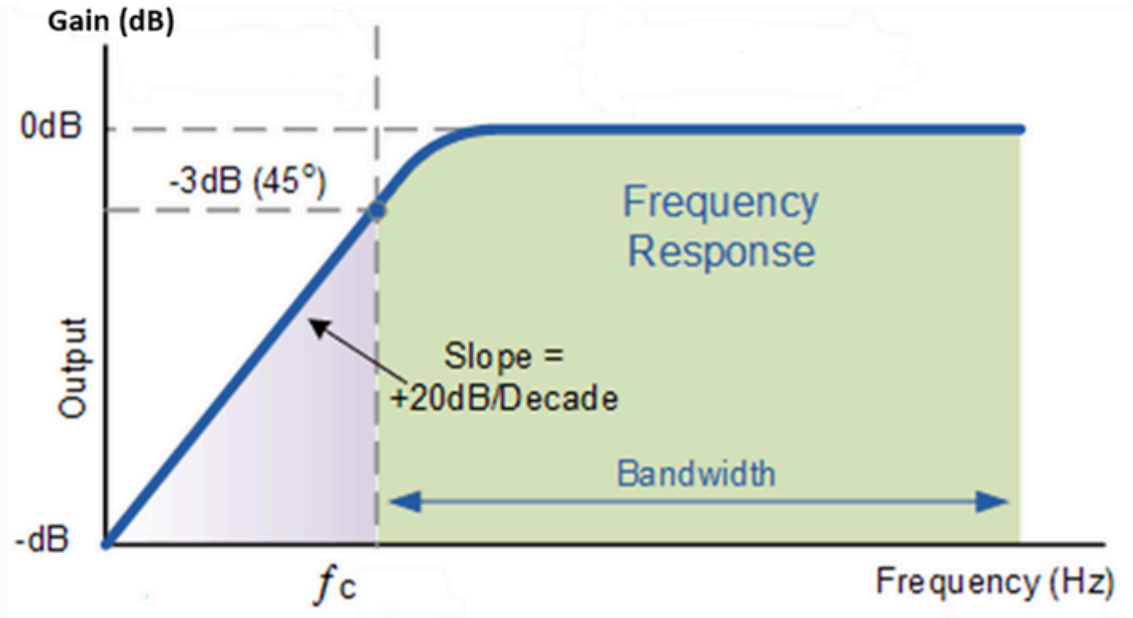
PASSIVE HIGH PASS FILTER

2.HIGH PASS CUT OFF FREQUENCY, FC:

The cutoff frequency of a high-pass filter is the frequency at which the output (load) voltage equals 70.7% of the input (source) voltage. Above the cutoff frequency, the output voltage is greater than 70.7% of the input. Below the cutoff frequency, the output voltage drops below 70.7%.

PHASE SHIFT ANGLE IS -45

$$f_{cutoff} = \frac{1}{2\pi RC}$$

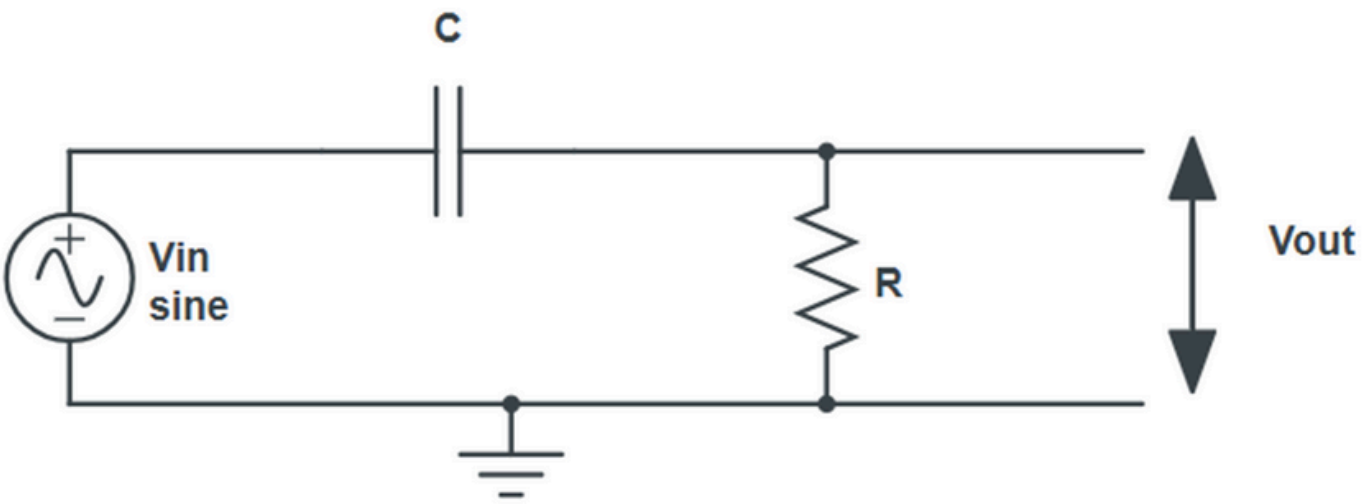


The gain-magnitude frequency response

PASSIVE HIGH PASS FILTER

3.**BASIC CIRCUIT** OF HIGH PASS FILTER CIRCUIT:

Also known as **first-order high pass filter**.

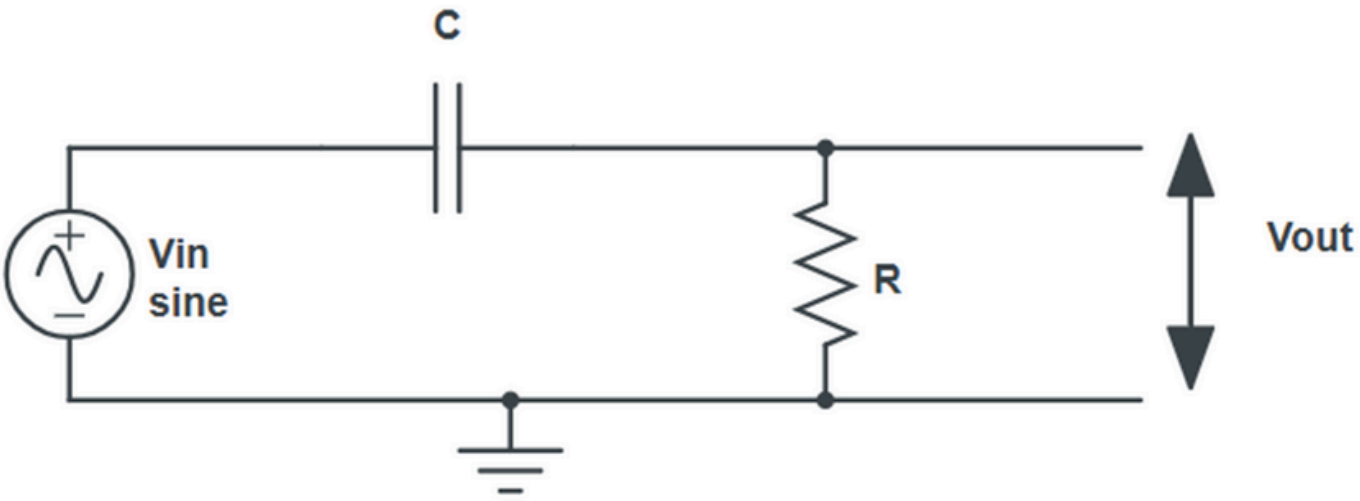


$$f_c = \frac{1}{2\pi RC}$$

$$A_V = \frac{V_{output}}{V_{input}}$$

$$A_{V(dB)} = 20 \log A_V$$

PASSIVE HIGH PASS FILTER



$$V_{out} = V_{in} \times \frac{R}{\sqrt{R^2 + X_c^{\,2}}}$$

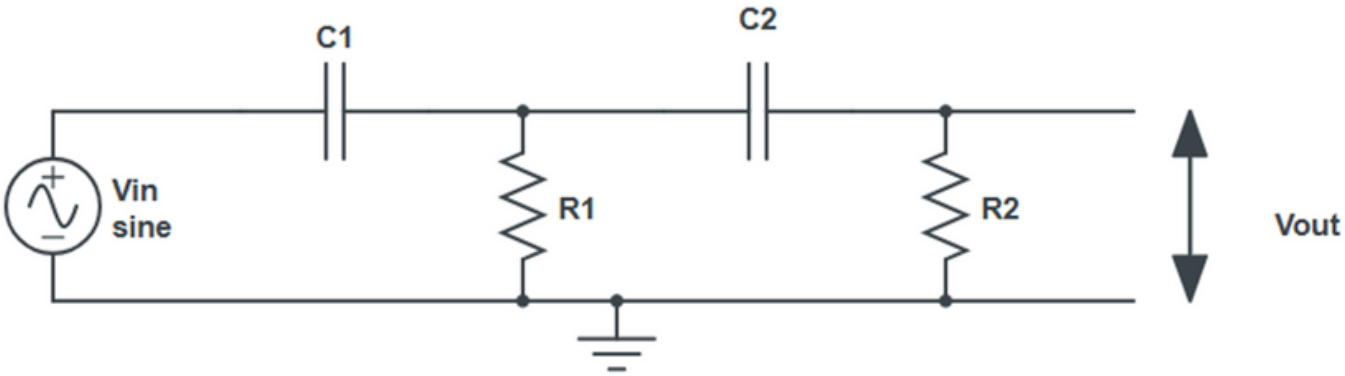
$$X_C = \frac{1}{2\pi f C} \text{ in Ohm's}$$

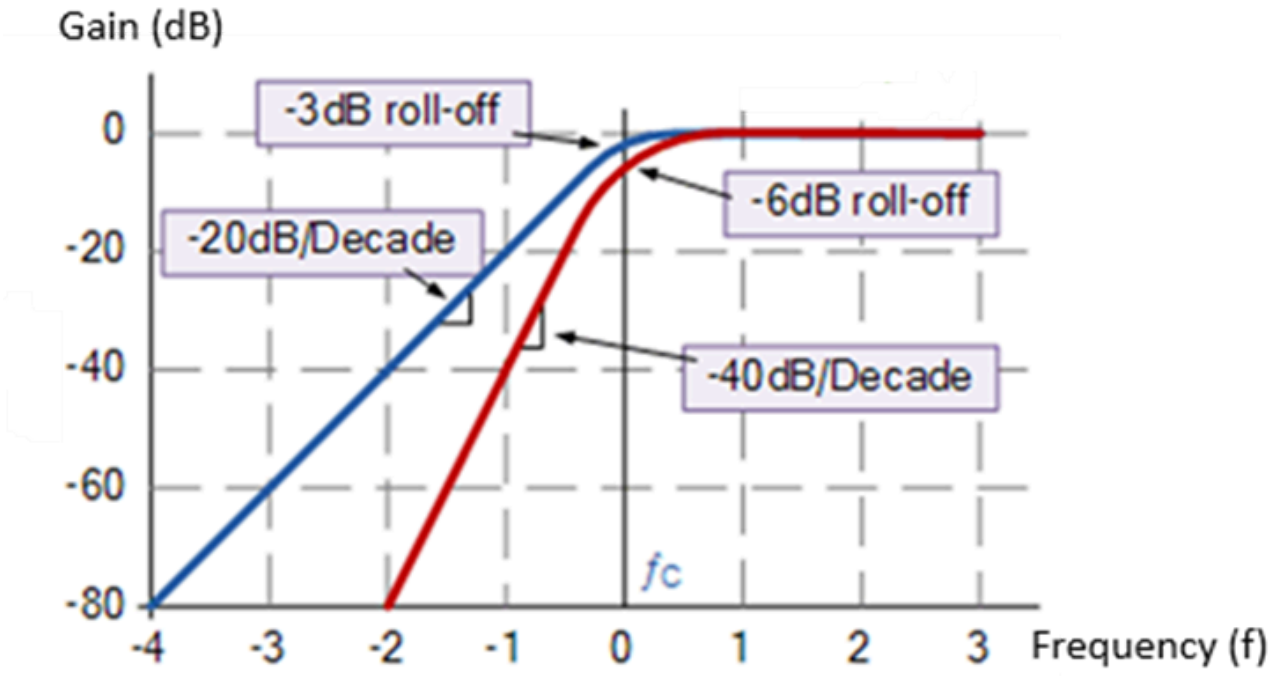
$$Z = \sqrt{R^2 + X_C^2}$$

PASSIVE HIGH PASS FILTER

CASCADED HIGH PASS FILTER CIRCUIT:

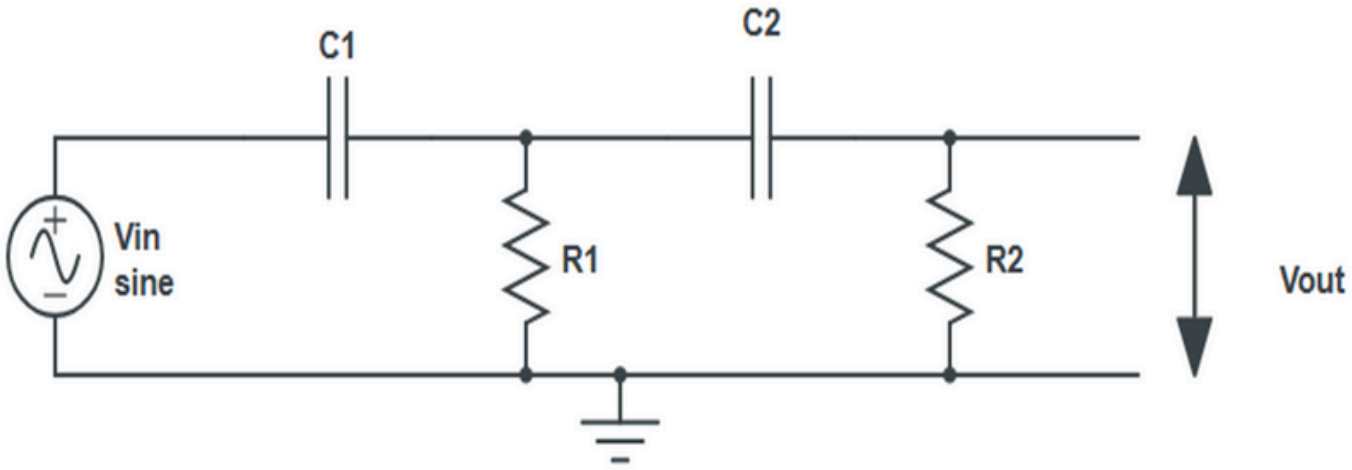
Also known as **second-order high pass filter.**





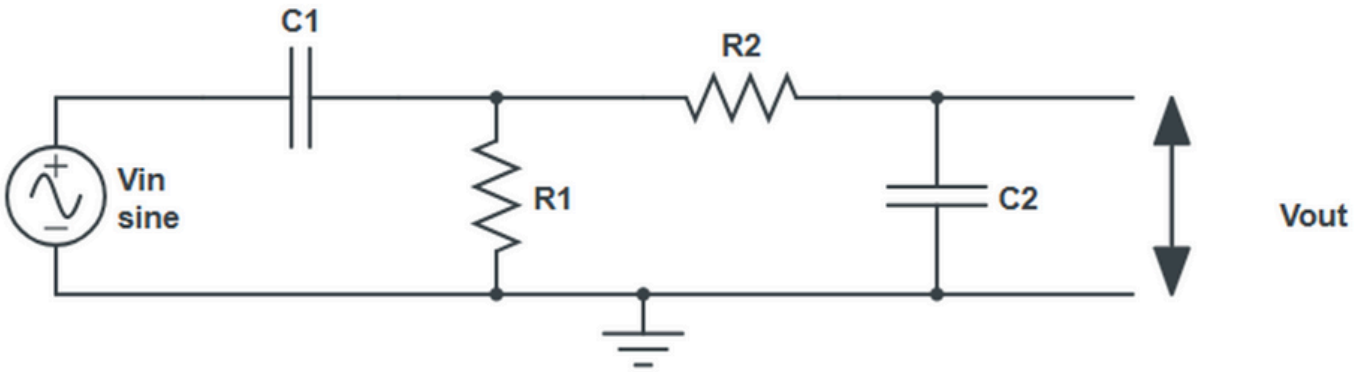
The gain-magnitude frequency response

PASSIVE HIGH PASS FILTER



$$f_C = \frac{1}{2\pi\sqrt{R_1 C_1 R_2 C_2}} \text{ Hz}$$

PASSIVE BAND PASS FILTER

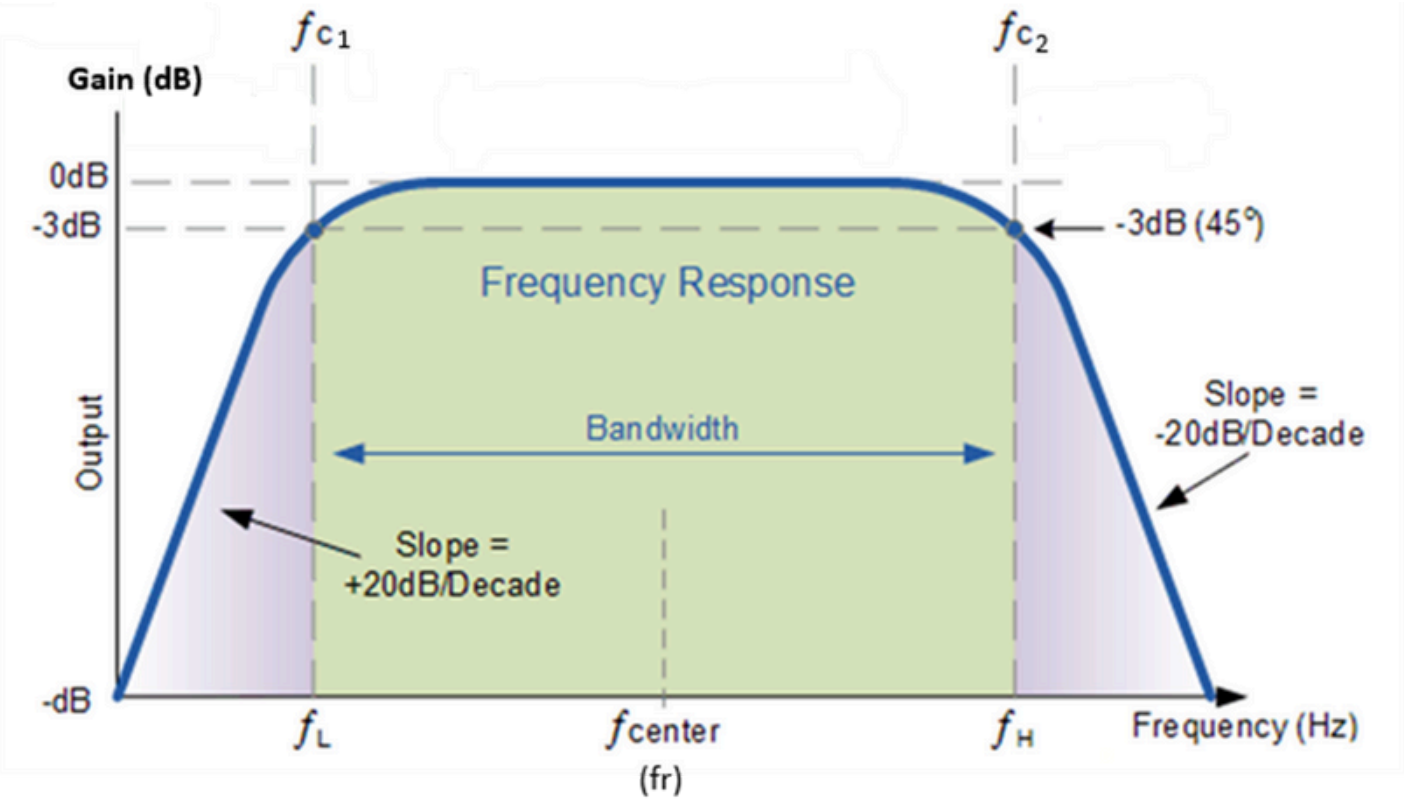


BAND PASS FILTER CIRCUIT

PASSIVE BAND PASS FILTER

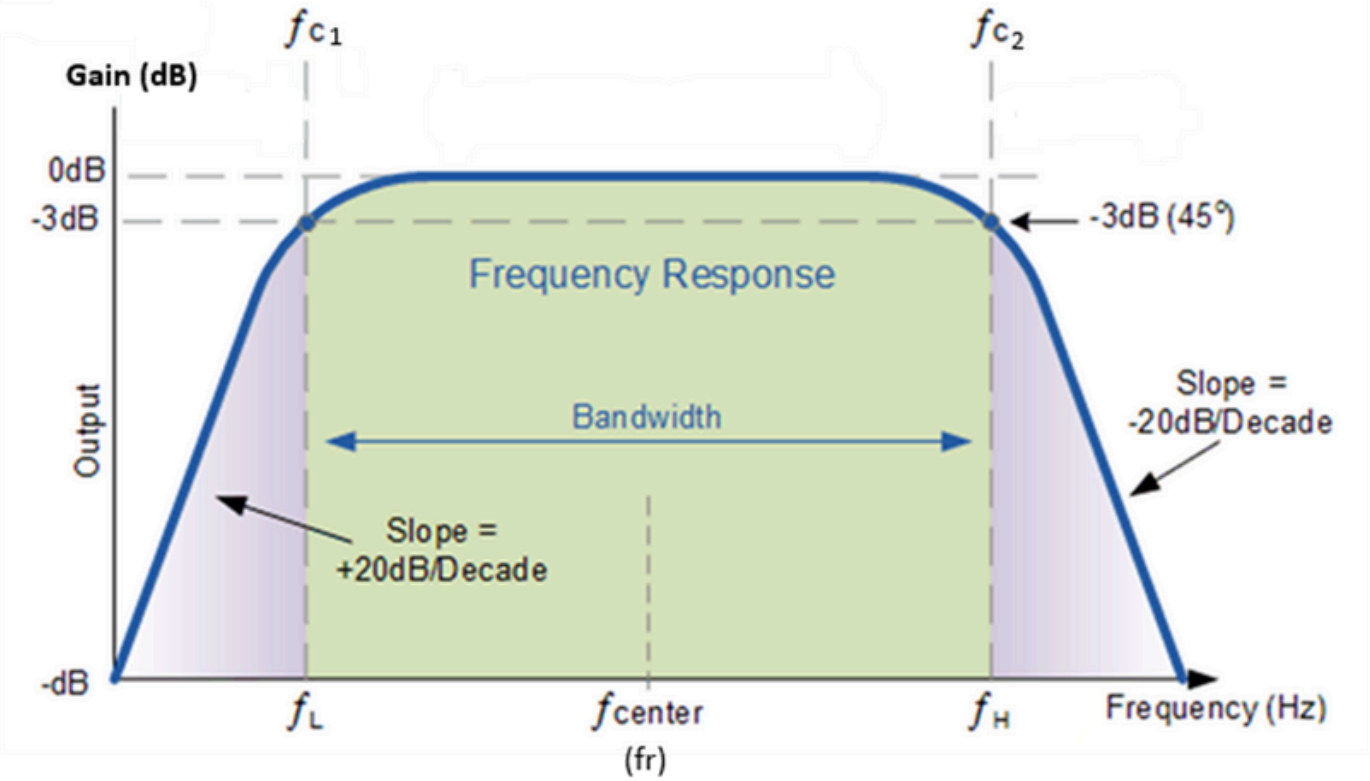
1.BAND PASS FILTER:

It allows signals within a specific frequency band between two cutoff (fc1- fc2) points to pass through, while blocking frequencies below and above this band.



The gain-magnitude frequency response

PASSIVE BAND PASS FILTER



The gain-magnitude frequency response

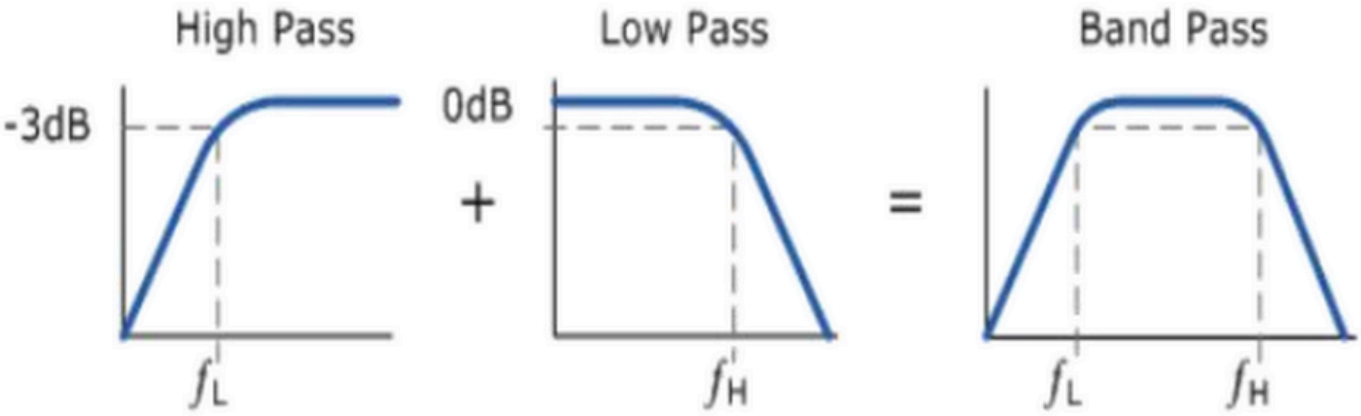
"Resonant" or "Centre Frequency" (*fr*) -point of the band pass filter were the output gain is at its maximum or peak value.

BW as being the difference between the lower cut-off frequency (fc_{LOWER}) and the higher cut-off frequency (fc_{HIGHER}) points.

PASSIVE BAND PASS FILTER

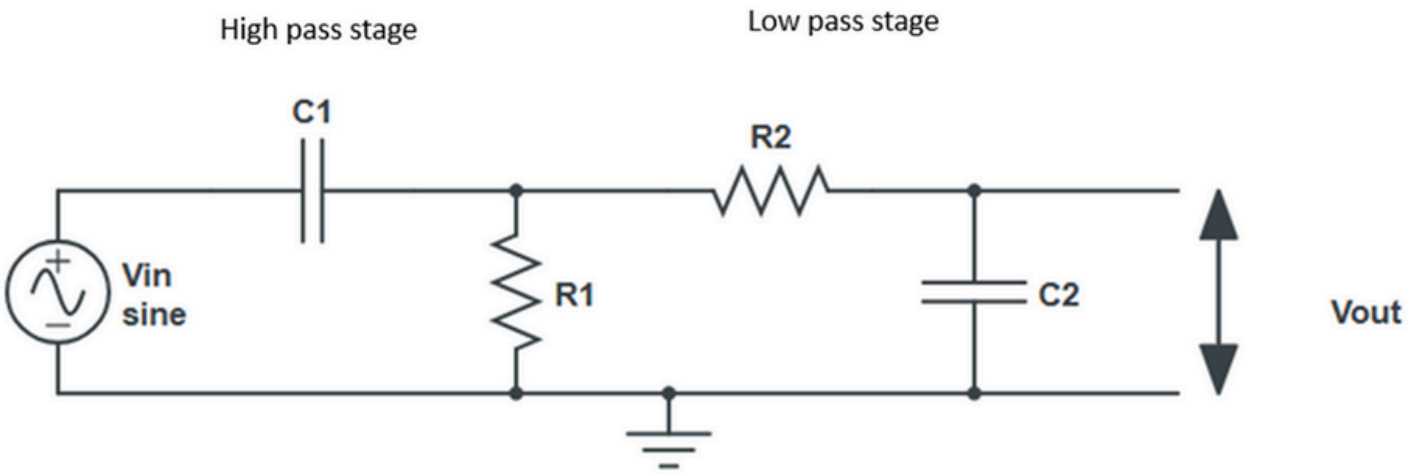
2.BAND PASS CUT OFF FREQUENCY, FC:

Where,
***f*r is the resonant or centre frequency**
***f*L is the lower -3dB cut-off frequency point**
***f*H is the upper -3db cut-off frequency point**



PASSIVE BAND PASS FILTER

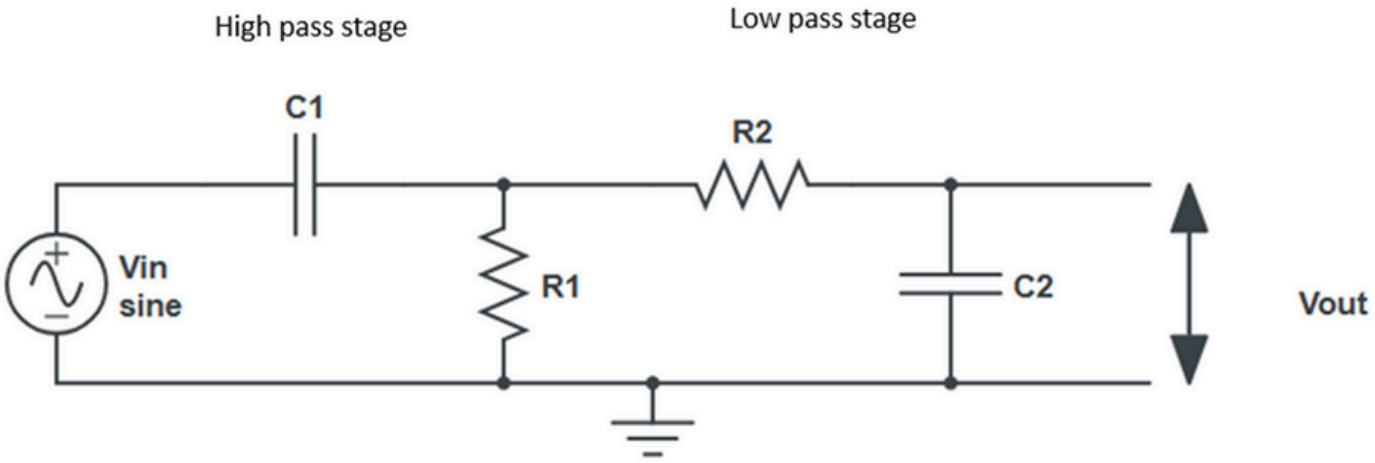
3.BAND PASS FILTER CIRCUIT.

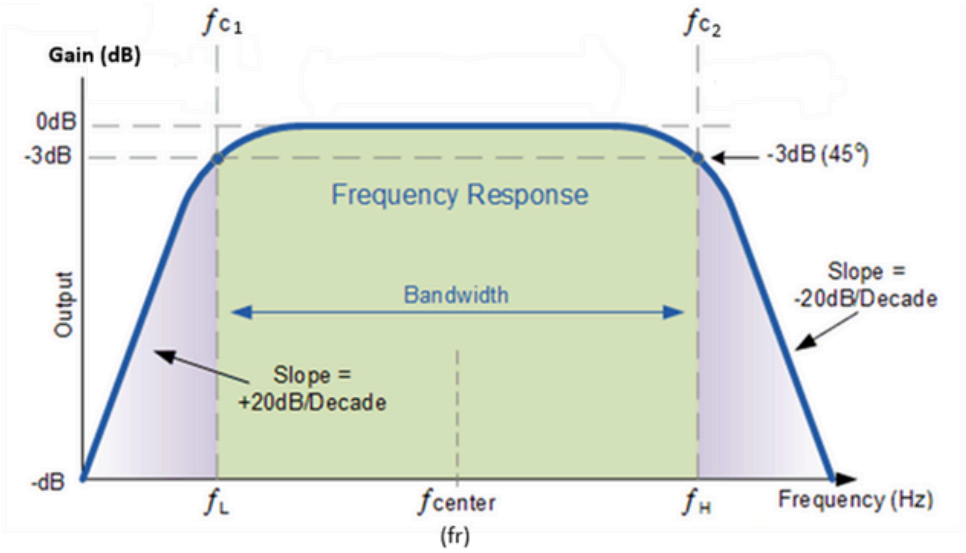


$$A_V = \frac{V_{output}}{V_{input}}$$

$$A_{V(dB)} = 20 \log A_V$$

PASSIVE BAND PASS FILTER





The gain-magnitude frequency response

$$f_L = \frac{1}{2\pi R_2 C_2}$$

$$f_H = \frac{1}{2\pi R_1 C_1}$$

$$fr = \sqrt{f_L \; x \; f_H}$$

$$BW = f_H - f_L$$

ACTIVE FILTER

TYPES OF ACTIVE FILTER

LOW-PASS FILTER

- Combining a basic RC Low Pass Filter circuit with an operational amplifier.
- First-order active low pass filter
- Second-order active low pass filter.

HIGH-PASS FILTER

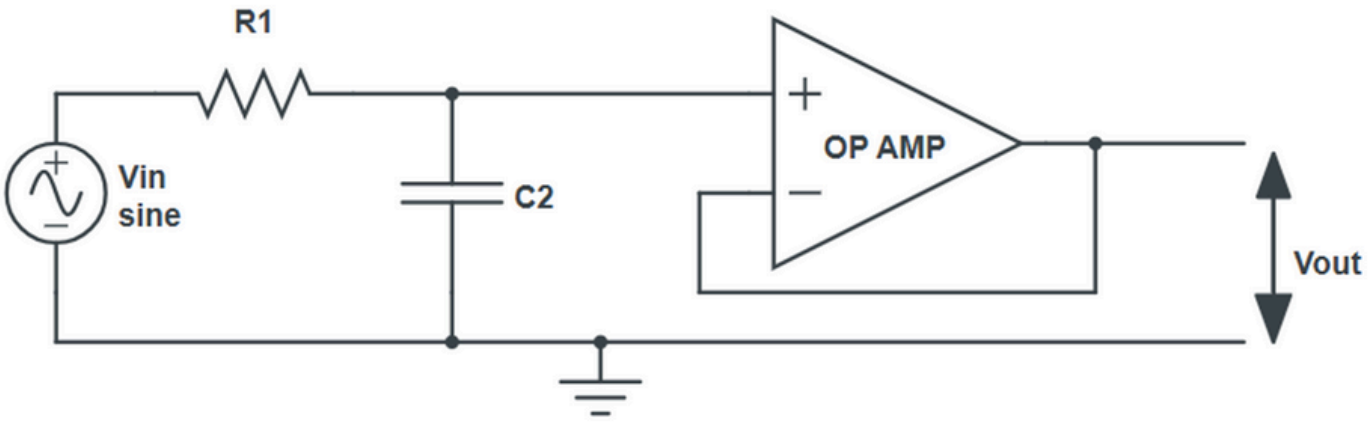
- Combining a basic RC High Pass Filter circuit with an operational amplifier.
- First-order active high pass filter
- Second-order active High pass filter

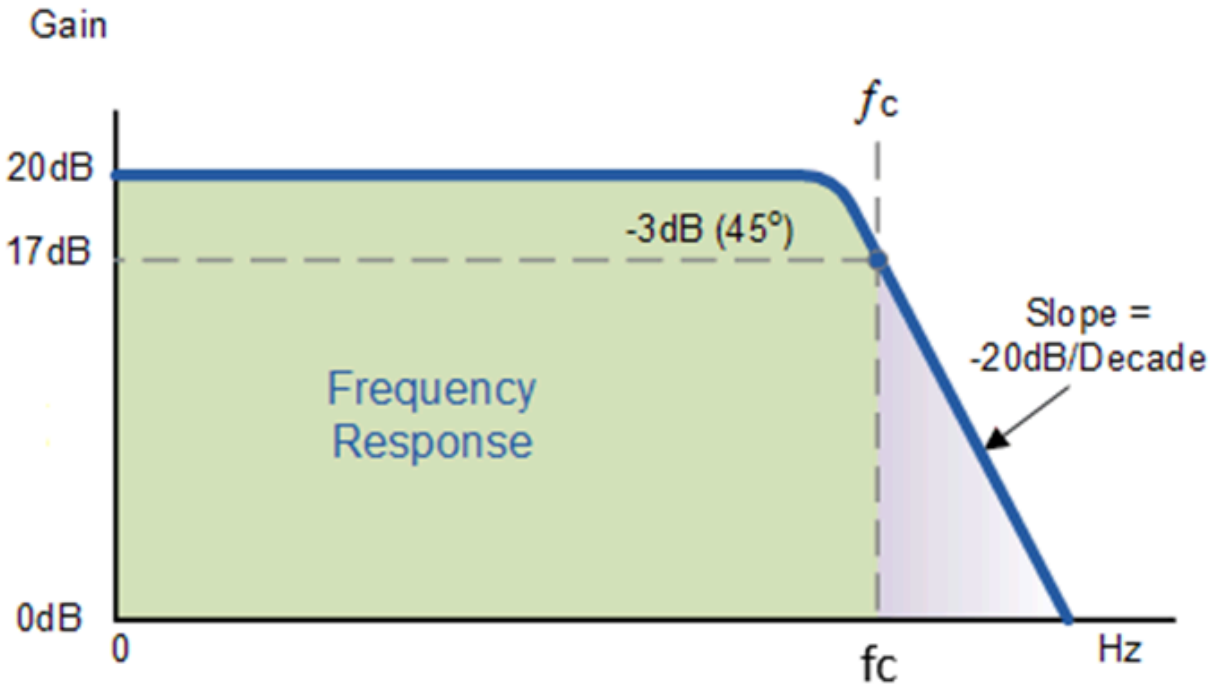
BAND-PASS FILTER

- Combining a basic Low Pass Filter circuit, High Pass Filter Circuit connected with an operational amplifier.

ACTIVE LOW PASS FILTER

1.Combining a basic RC Low Pass Filter circuit with an operational amplifier.

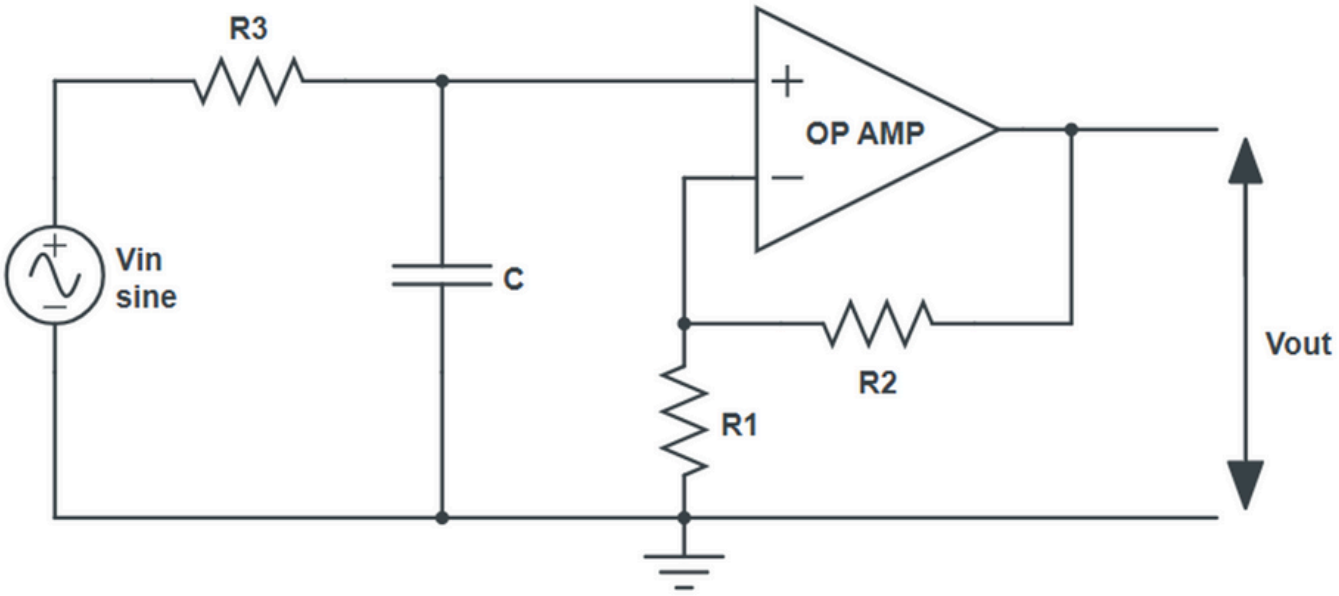




The gain-magnitude frequency response

ACTIVE LOW PASS FILTER

2. FIRST-ORDER ACTIVE LOW PASS FILTER.



$$Av(dB) = 20\log_{10}\left(\frac{Vout}{Vin}\right)$$

$$\therefore -3dB = 20\log_{10}\left(0.707\,\frac{Vout}{Vin}\right)$$

$$f_{cutoff} = \frac{1}{2\pi RC}$$

$$\text{DC gain} = \left(1 + \frac{R_2}{R_1}\right)$$

ACTIVE LOW PASS FILTER

$$Voltage\ Gain,\ (Av) = \frac{Vout}{Vin} = \frac{A_F}{\sqrt{1 + \left(\frac{f}{fc}\right)^2}}$$

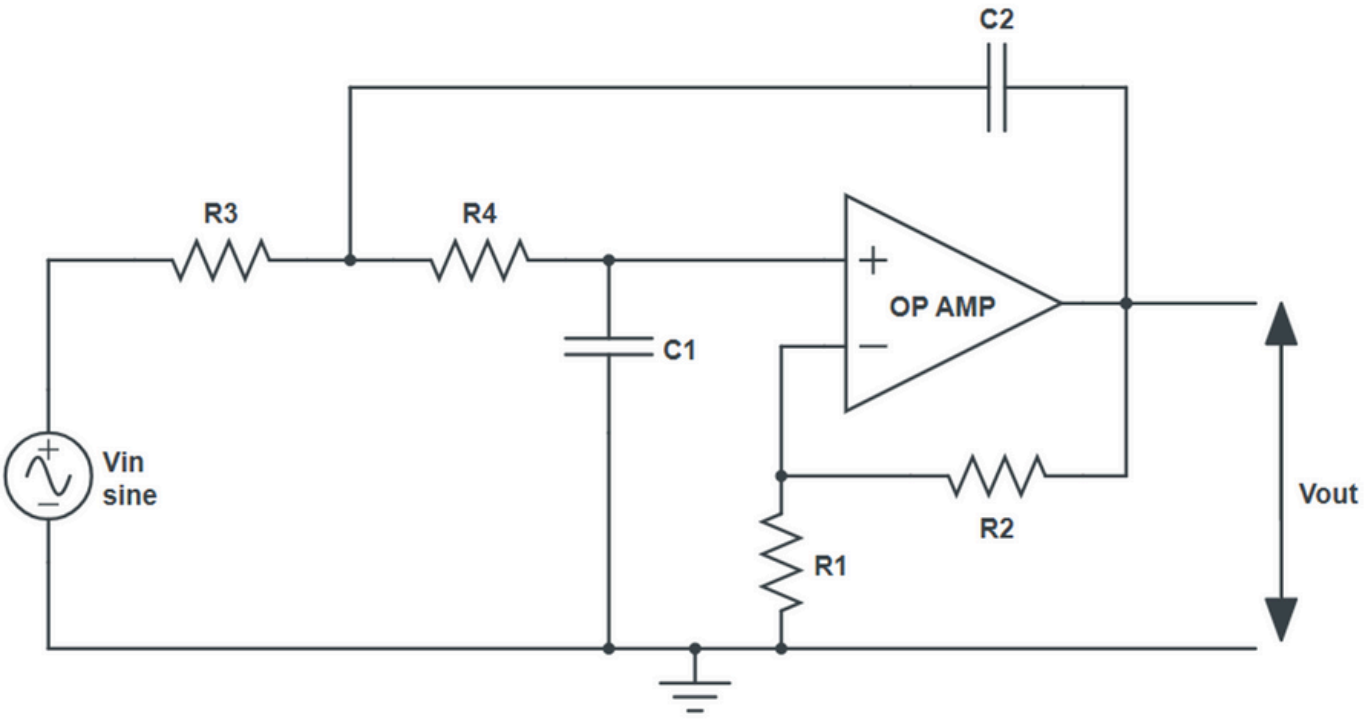
A_F = the pass band gain of the filter, (1 + R2/R1)

f = the frequency of the input signal in Hertz, (Hz)

fc = the cut-off frequency in Hertz, (Hz)

ACTIVE LOW PASS FILTER

3. SECOND-ORDER ACTIVE LOW PASS FILTER.

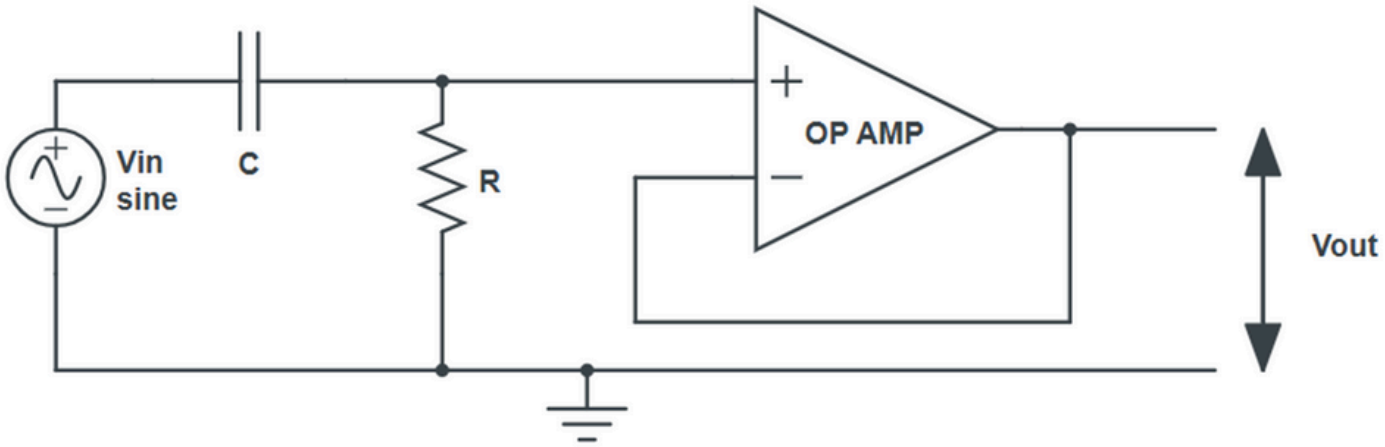


$$f_c = \frac{1}{2\pi\sqrt{R_3R_4C_1C_2}}$$

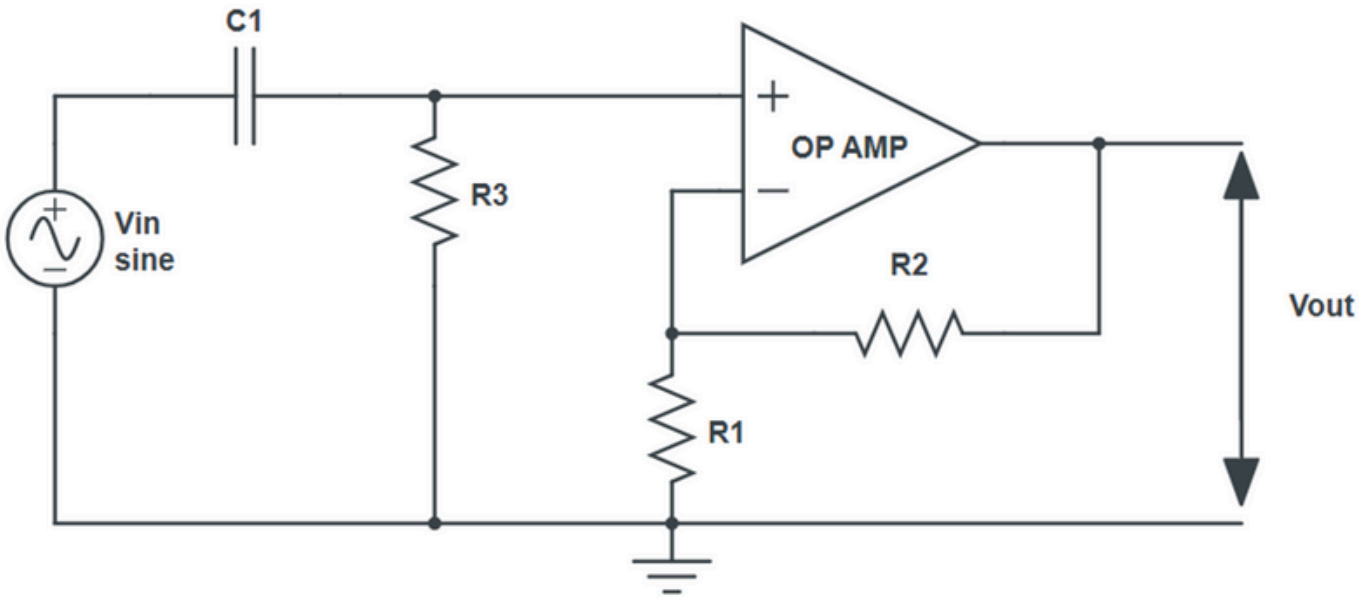
$$Av = 1 + \frac{R_2}{R_1}$$

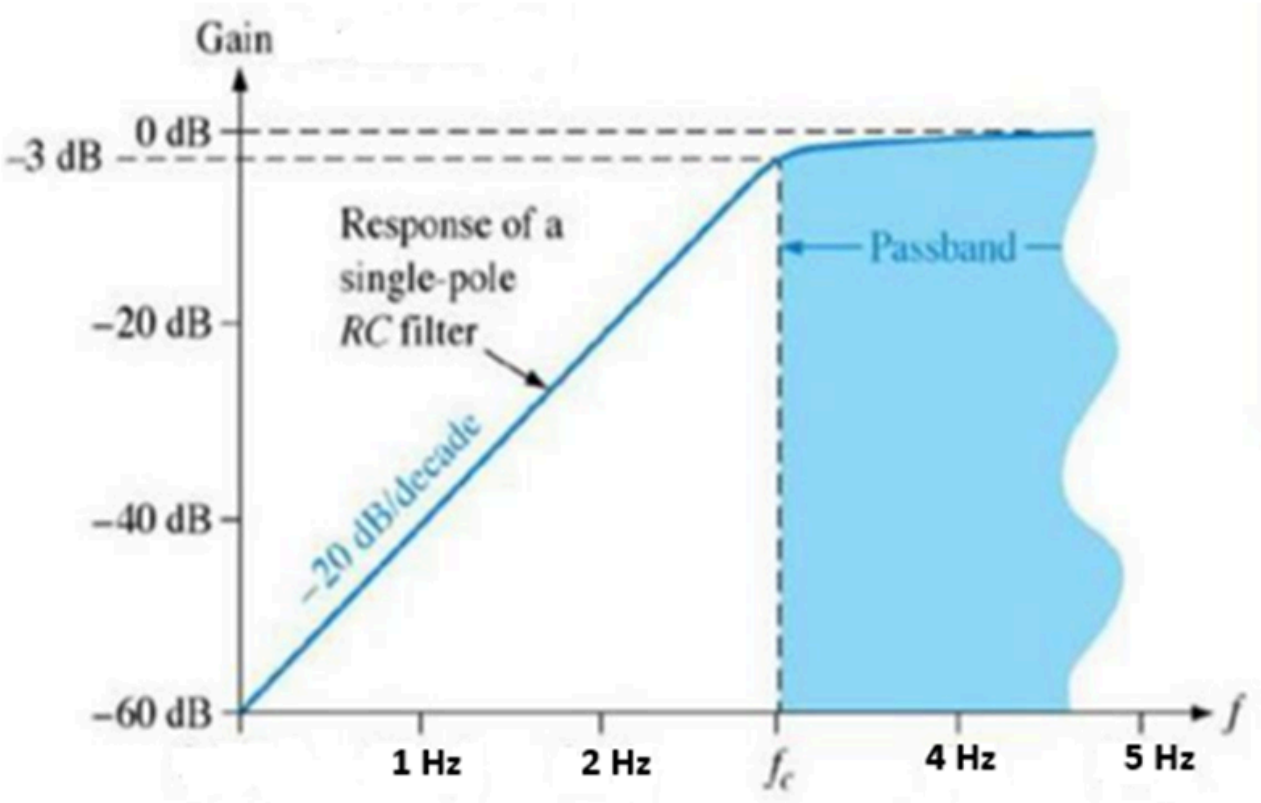
ACTIVE HIGH PASS FILTER

Combining a basic RC High Pass Filter circuit with an operational amplifier.



ACTIVE HIGH PASS FILTER

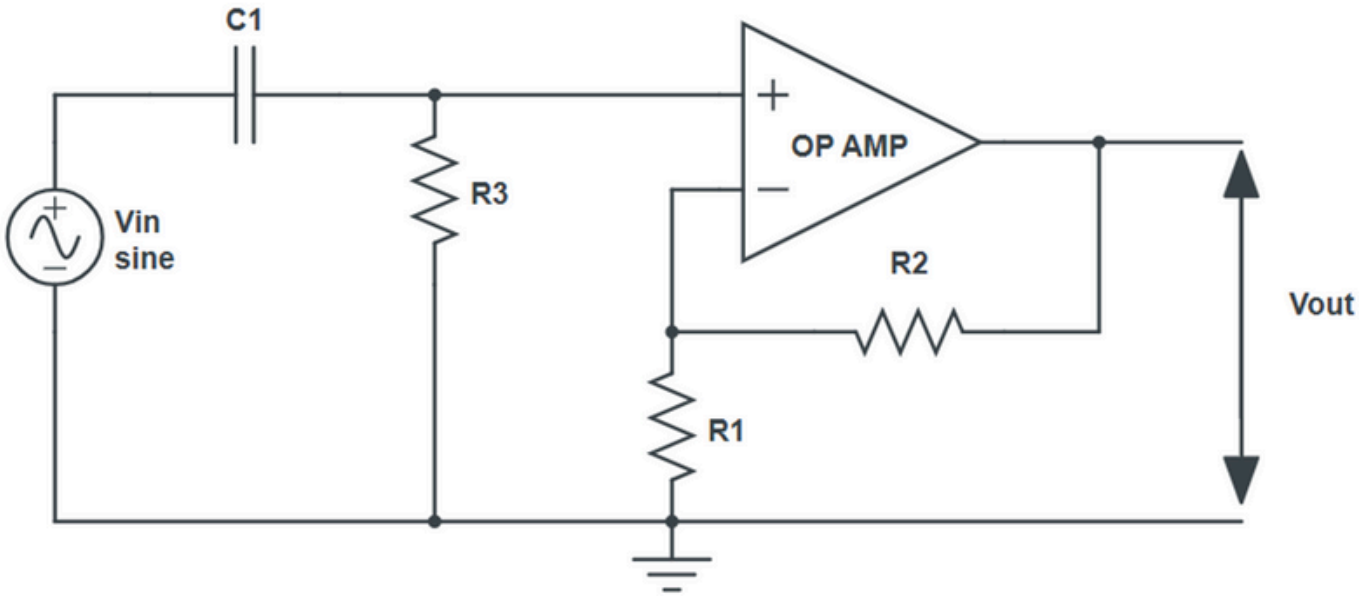




The gain-magnitude frequency response

ACTIVE HIGH PASS FILTER

2. FIRST-ORDER ACTIVE HIGH PASS FILTER.



$$Av(dB) = 20\log_{10}\left(\frac{Vout}{Vin}\right)$$

$$\therefore -3dB = 20\log_{10}\left(0.707\,\frac{Vout}{Vin}\right)$$

$$f_{cutoff} = \frac{1}{2\pi RC}$$

$$\text{DC gain} = \left(1 + \frac{R_2}{R_1}\right)$$

ACTIVE HIGH PASS FILTER

$$\text{Voltage Gain, (Av)} = \frac{\text{Vout}}{\text{Vin}} = \frac{A_F\left(\frac{f}{fc}\right)}{\sqrt{1+\left(\frac{f}{fc}\right)^2}}$$

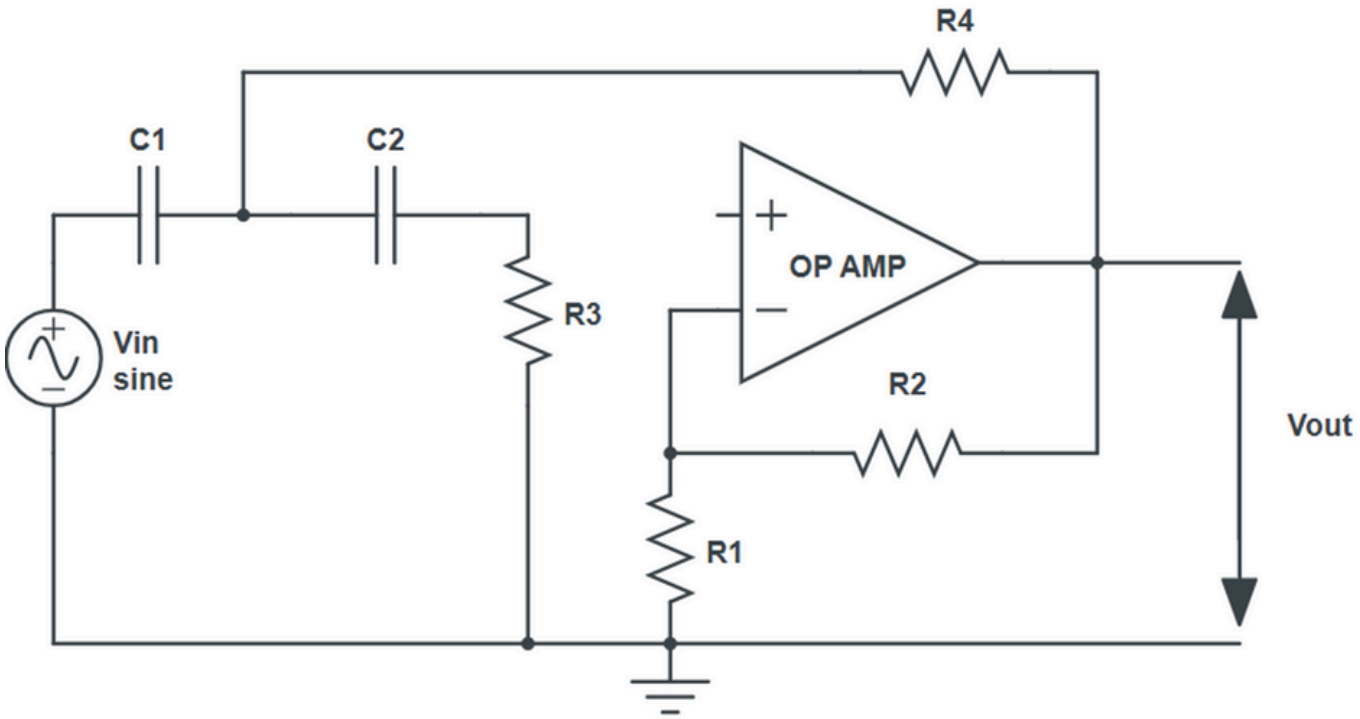
A_F = the pass band gain of the filter, (1 + R2/R1)

f = the frequency of the input signal in Hertz, (Hz)

fc = the cut-off frequency in Hertz, (Hz)

ACTIVE HIGH PASS FILTER

3. SECOND-ORDER ACTIVE HIGH PASS FILTER.

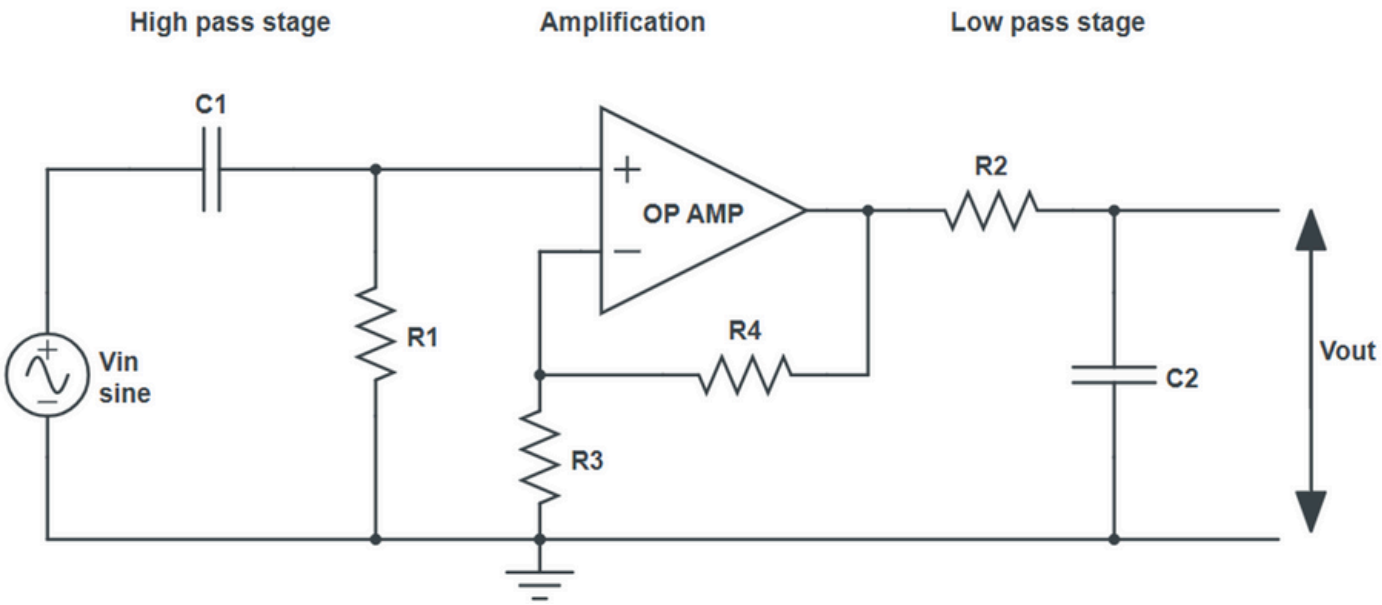


$$f_c = \frac{1}{2\pi\sqrt{R_3R_4C_1C_2}}$$

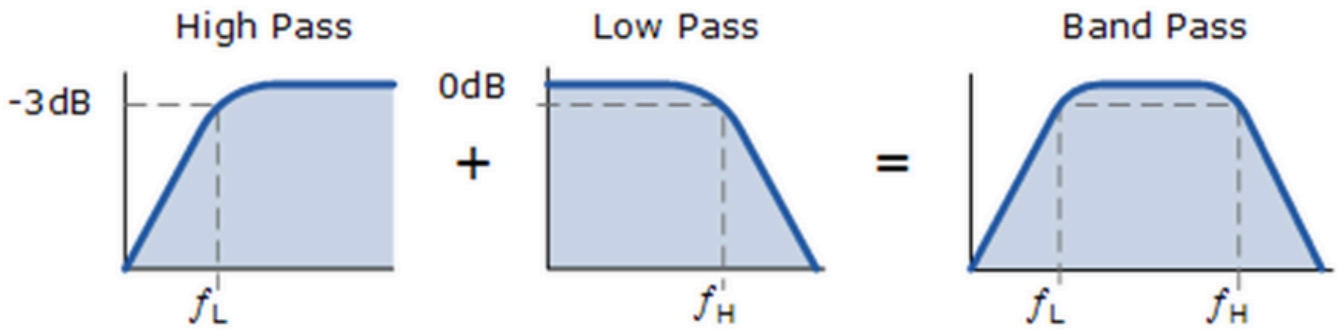
$$Av = 1 + \frac{R_2}{R_1}$$

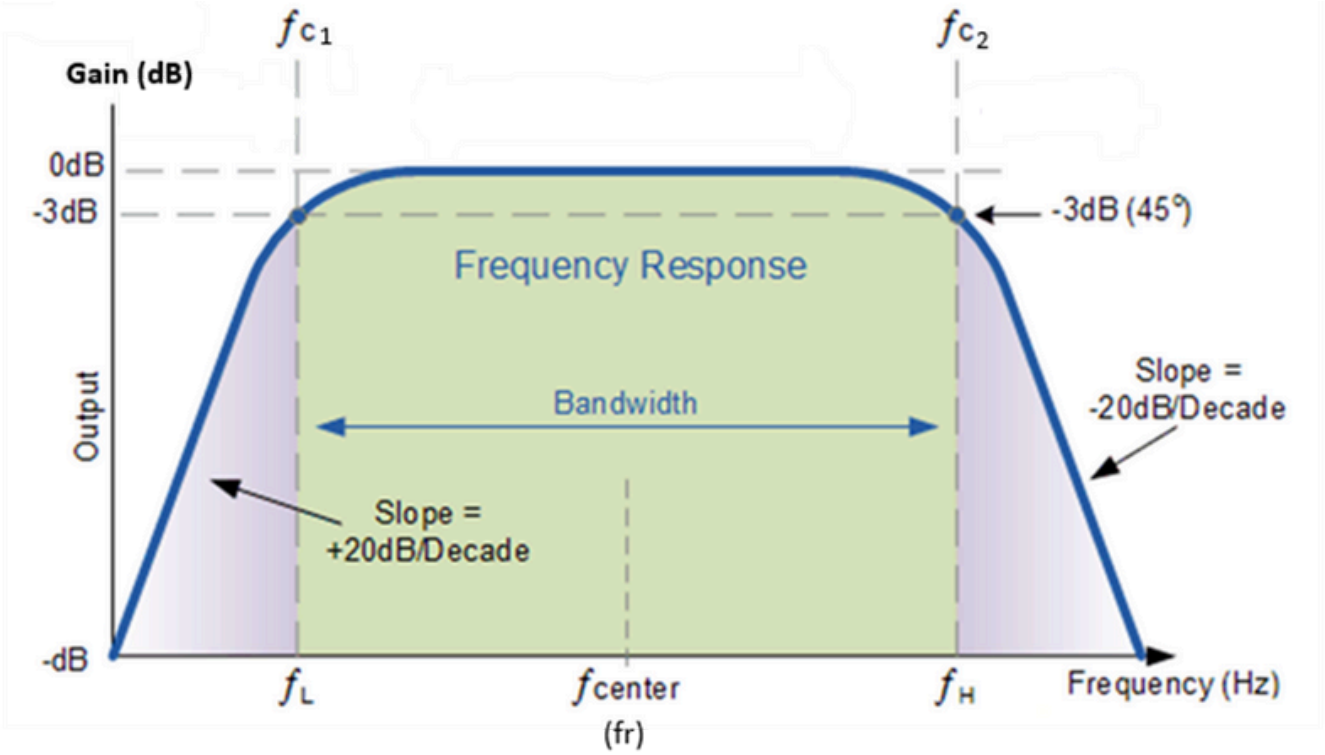
ACTIVE BAND PASS FILTER

1.Combining a basic Low Pass Filter circuit, High Pass Filter Circuit connected with an operational amplifier.



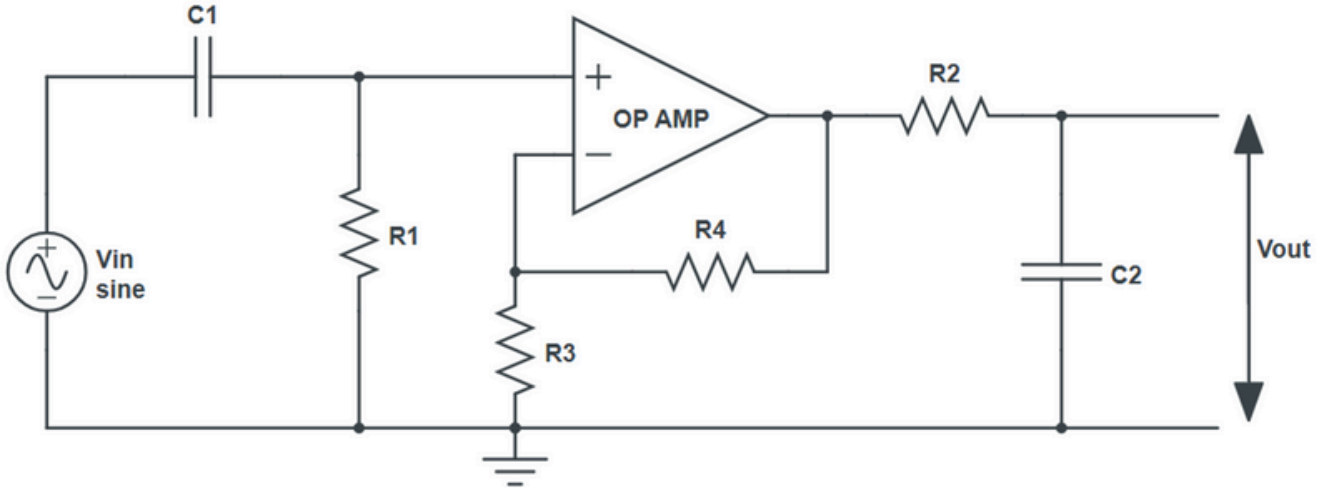
ACTIVE BAND PASS FILTER





The gain-magnitude frequency response

ACTIVE BAND PASS FILTER



CUT-OFF FREQUENCY

SCAN ME

$$AV = 1 + \frac{R4}{R3}$$

$$fc_1 = \frac{1}{2\pi R_1 C_1}, \quad fc_2 = \frac{1}{2\pi R_2 C_2}$$

$$f_r = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$$

$$fr = \sqrt{f_L \; x \; f_H}$$

EXERCISE

1. THREE (3) main types of filters are low-pass, high-pass and band-pass. Explain clearly the function of each filter.
2. Compare Three (3) differences between Passive and Active Filter circuits.
3. Explain the operation of Passive Low Pass Filter by using aided diagram.
4. State THREE (3) types of passive filter.
5. Passive filter will accept or reject certain frequencies of signal. Sketch and label the complete frequency response curves for passive Low Pass and High Pass Filters.
6. Describe THREE (3) characteristic of passive and active filters.
7. State THREE (3) types of active filter.
8. Explain the operation of Passive High Pass Filter by using aided diagram.

EXERCISE

1. Calculate the lower and upper cut-off frequencies of the band pass filter circuit below. (FE S1 2022/2023).

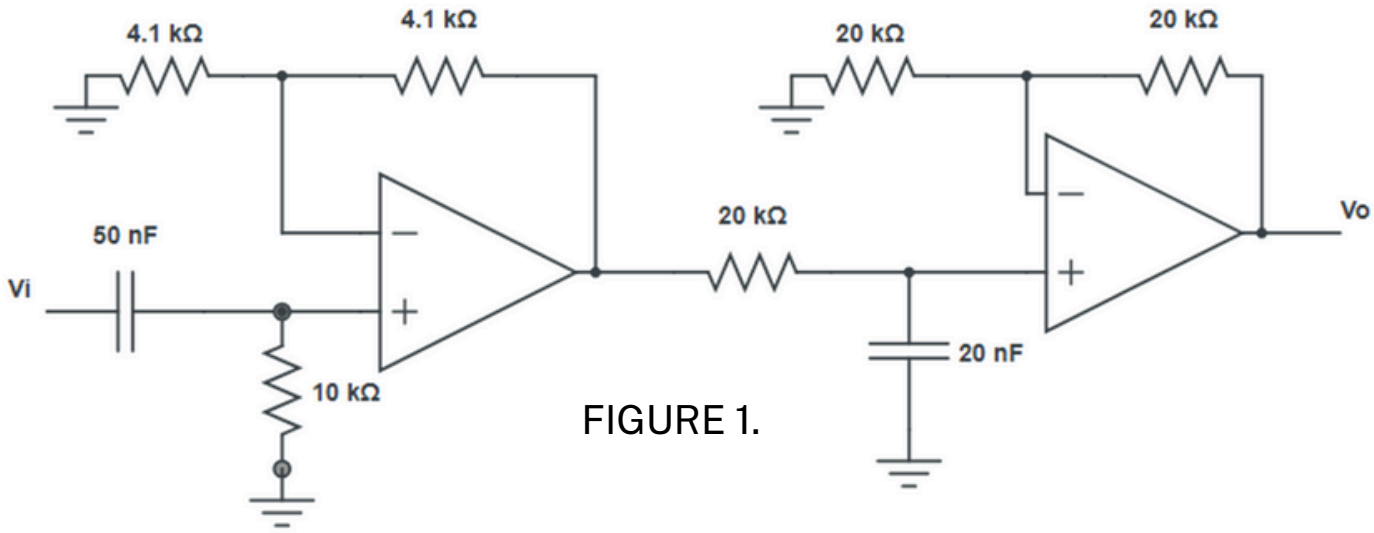


FIGURE 1.

ANSWER:

$$lower\ cut-off\ freq, \quad Fc1 = \frac{1}{2\pi RC}$$

$$= \frac{1}{2\pi(10K)(50n)}$$

$$= 318.31\text{Hz}$$

$$upper\ cut-off\ freq, \quad Fc2 = \frac{1}{2\pi RC}$$

$$= \frac{1}{2\pi(20K)(20n)}$$

$$= 397.88\text{Hz}$$

EXERCISE

2. Based on figure 2 below, sketch the ideal frequency response second order high pass active filter and calculate the cut off frequency and voltage gain. (FE S1 2023/2024)

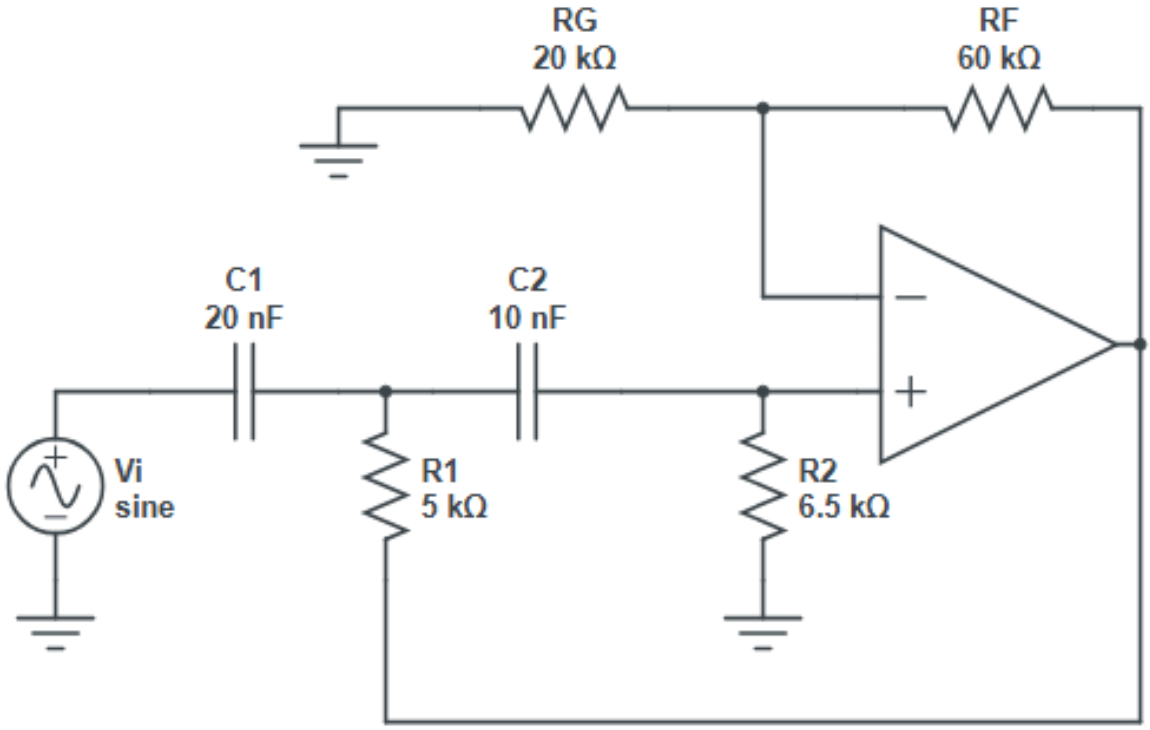
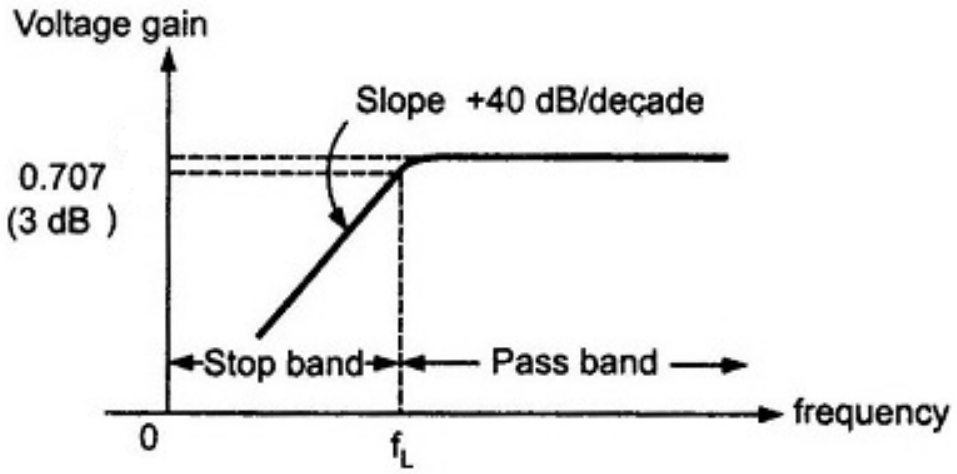


FIGURE 2.

ANSWER:



EXERCISE

$$\text{Cut} - \text{off freq, Fc} = \frac{1}{2\pi\sqrt{R1C1R2C2}}$$

$$= \frac{1}{2\pi\sqrt{(5K)(20nF)(6.5K)(10nF)}}$$

$$= 1.97KHz$$

$$\text{Voltage gain, Vout} = 1 + \frac{Rf}{Rg}$$

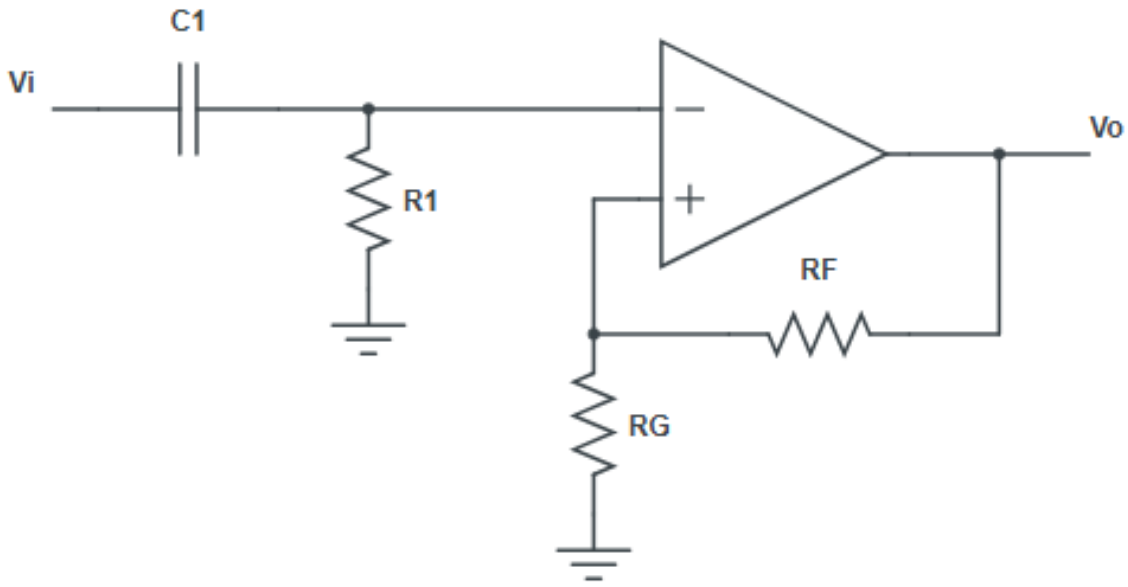
$$= 1 + \frac{60K}{20K}$$

$$= 4$$

EXERCISE

3. With the aid of a suitable diagram, calculate the cut off frequency, fc point of inverting active high pass filter, with the R=150KΩ and the capacitor C=2.2PF. (FE S2 2023/2024)

ANSWER:



$$Cut-off\ freq, \qquad Fc = \frac{1}{2\pi RC}$$

$$= \frac{1}{2\pi(150K)(2.2pF)}$$

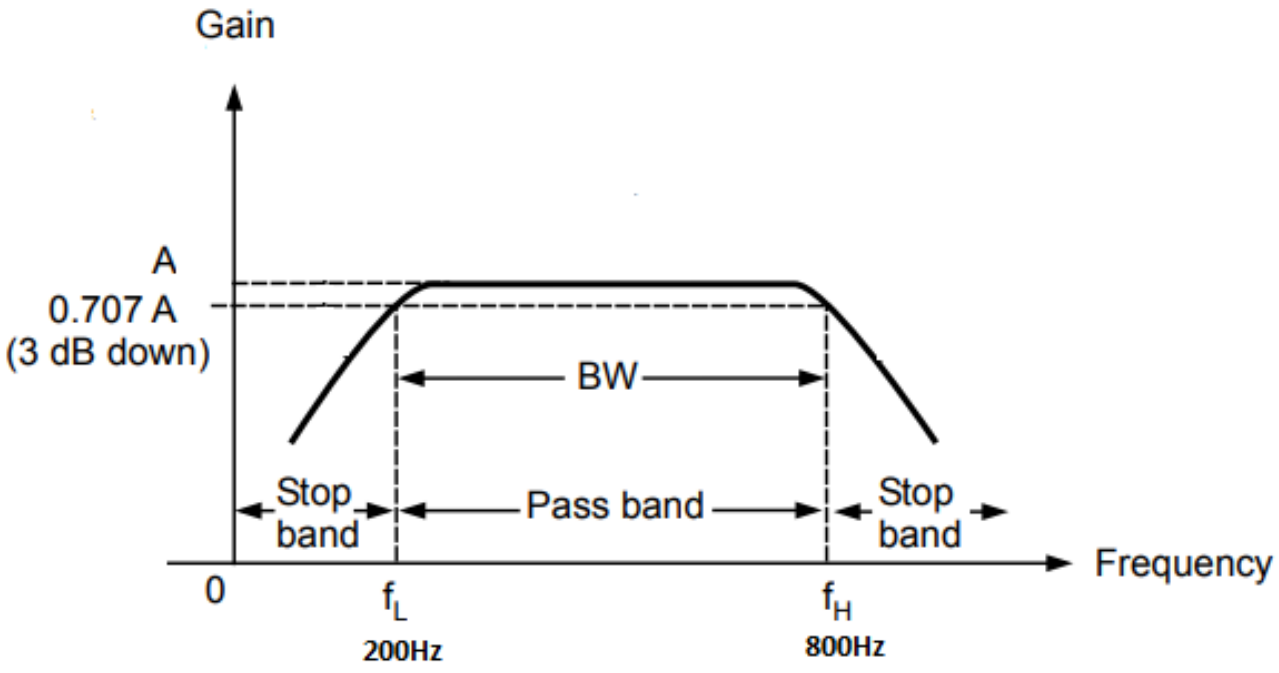
$$= 482\text{KHz}$$

EXERCISE

4. A band pass filter has a cut-off frequency of 200Hz, and an upper cut-off frequency of 800Hz. Sketch the frequency response curve of the filter to determine which frequency will pass through the filter and the bandwidth of this filter, if the input signal is a combination of frequencies 100Hz, 300Hz, 500Hz and 1000Hz. (FE S1 2024/2025)

ANSWER:

$$\text{Bandwidth, BW} = FH - FL$$



Freq:

1. 100Hz = blocked
2. 300Hz = passes
3. 500Hz = passes
4. 1000Hz = blocked

EXERCISE

5. Based on the figure 3 below, sketch the ideal frequency response for a second order high pass active filter and calculate the cut off frequency and voltage gain given that the value of C1=0.02uF, C2=0.01uF, R1=5KΩ, R2=6.5KΩ, R3=20KΩ and R4=60KΩ. (FE S2 2024/2025)

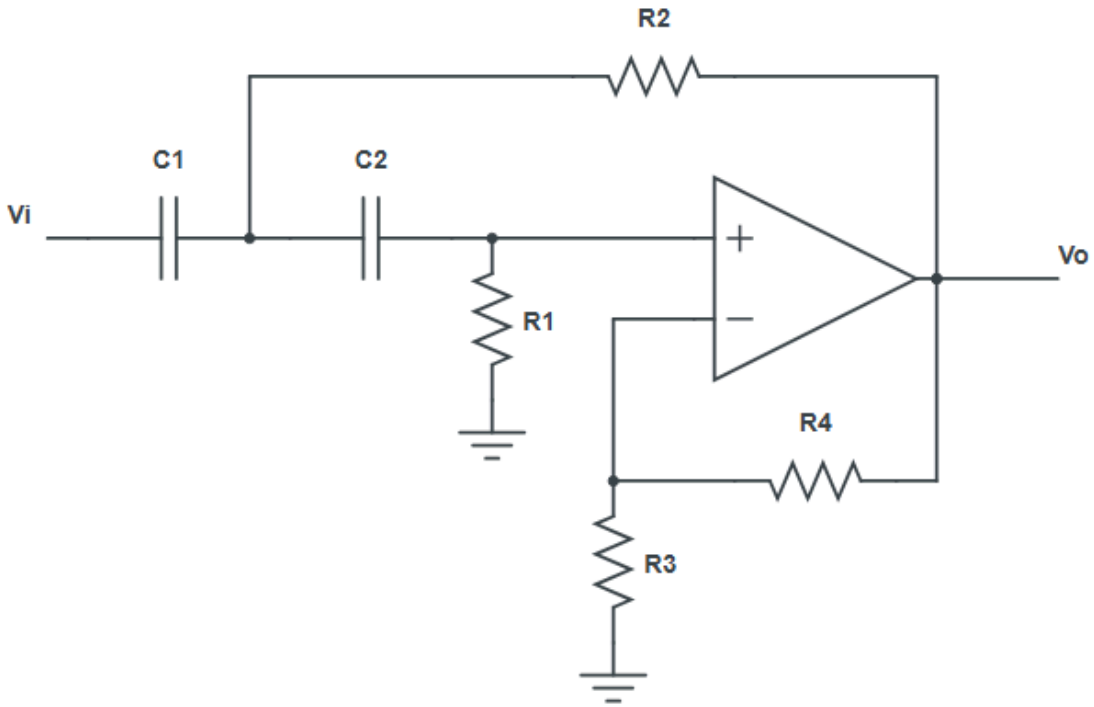
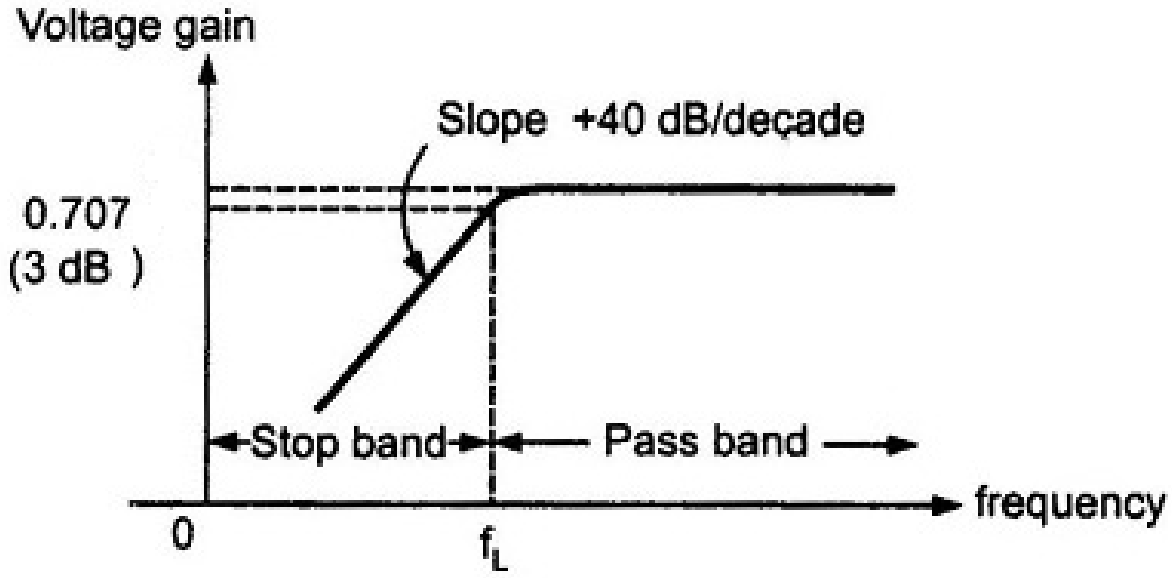


FIGURE 3.

ANSWER:

EXERCISE



$$Cut-off\ freq, \qquad Fc2 = \frac{1}{2\pi\sqrt{R1C1R2C2}}$$

$$= \frac{1}{2\pi\sqrt{(5K)(0.02uF)(6.5K)(0.01uF)}}$$

$$= 1.97\text{KHz}$$

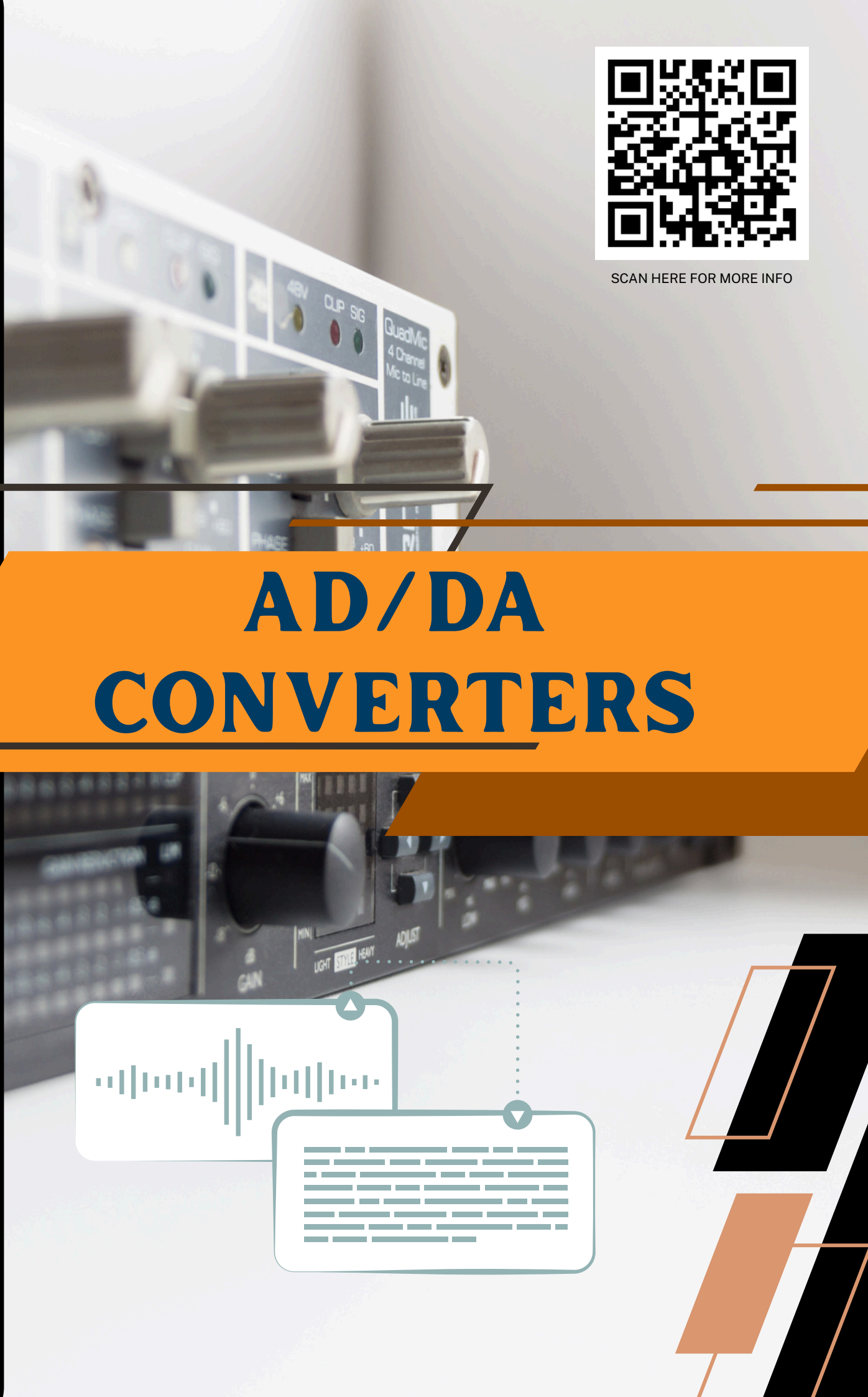
$$Voltage\ gain, \qquad AV = 1 + \frac{R4}{R3}$$

$$= 1 + \frac{60\ K}{20\ K}$$

$$= 4$$

SCAN HERE FOR MORE INFO

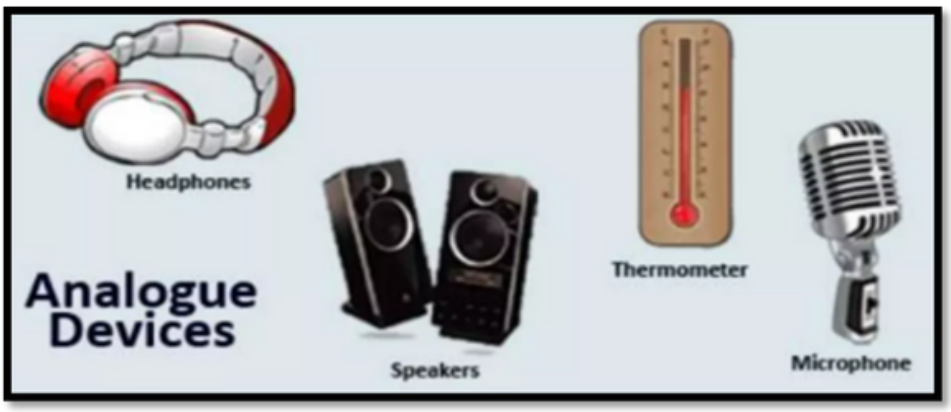
AD/DA CONVERTERS



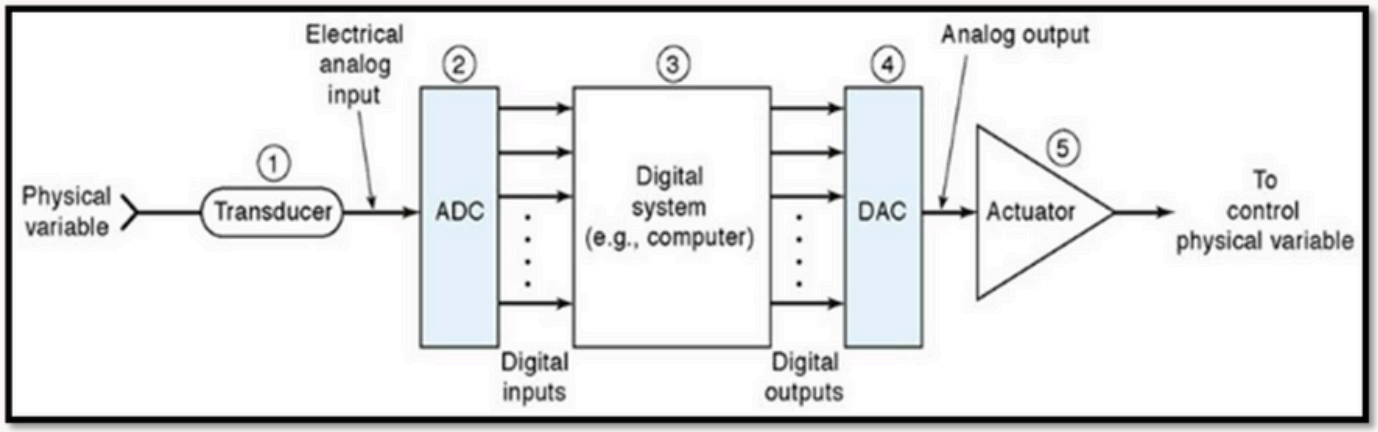
INTRODUCTION TO AD/DA CONVERTERS

Analogue-to-Digital Converters (ADC) and Digital-to-Analogue Converters (DAC) are essential components in modern electronic systems, bridging the gap between the analog real world and the digital domain used by computers and digital devices.

These converters enable accurate and reliable performance in a wide range of applications, including communications, energy, healthcare, instrumentation and measurement, motor and power control, industrial automation, aerospace and defense.

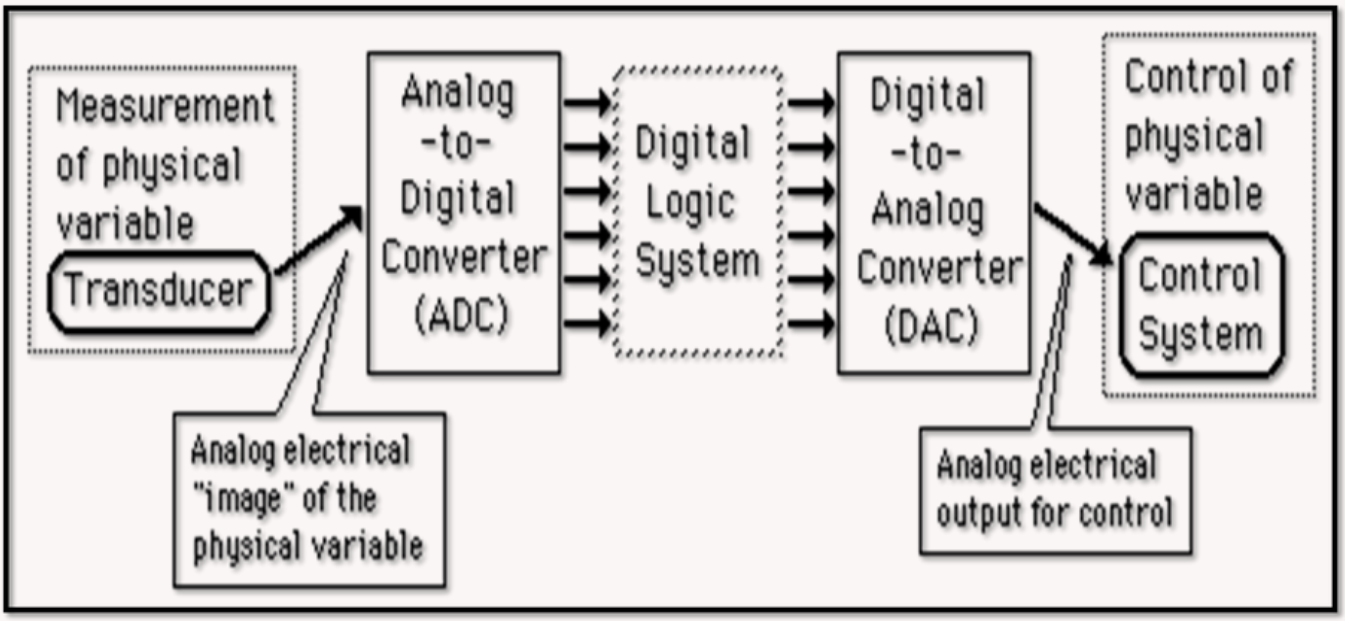


ADC AND DAC INTERFACE BETWEEN COMPUTERS



The system shows analogue to digital converter (ADC) and digital to analogue converter (DAC) serves as the interface between the digital and analogue systems.

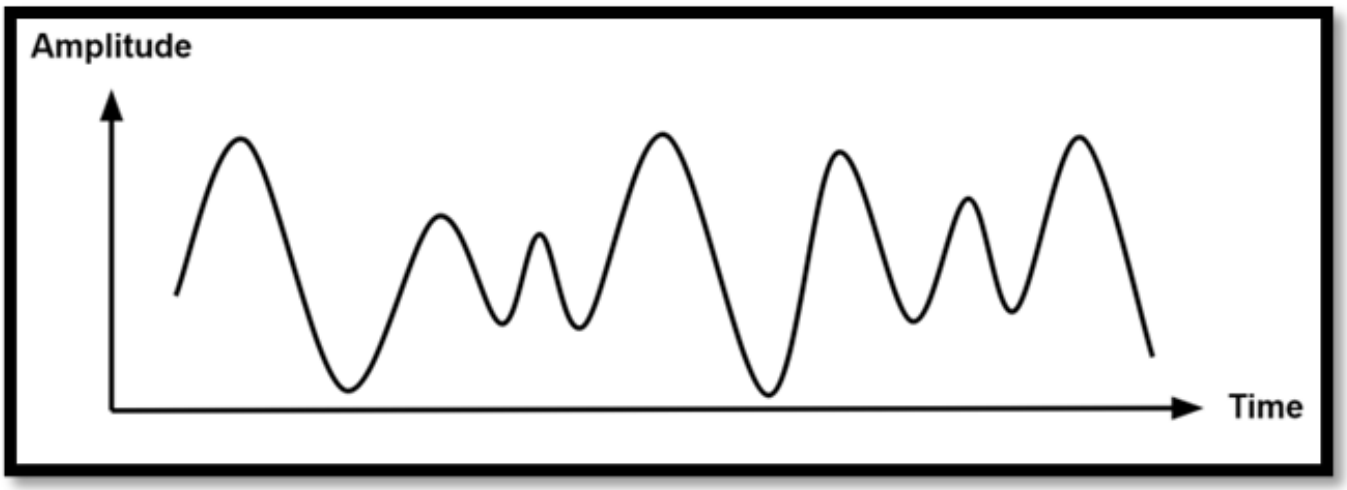
EXAMPLE ADC AND DAC APPLICATION: DATA COLLECTION AND CONTROL



The system shows analogue to digital converter (ADC) and digital to analogue converter (DAC) serves as the interface between the digital and analogue systems.

ANALOGUE SIGNALS

- An analogue signal is a continuous signal that represents some other varying quantity, such as sound, light, temperature, or pressure.



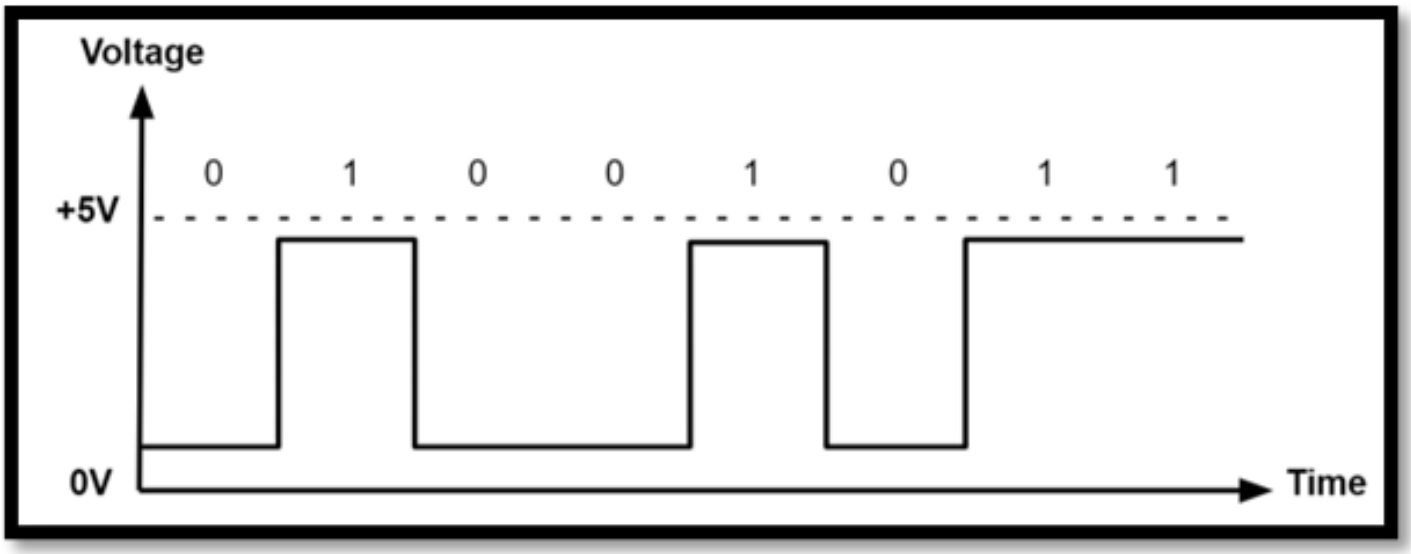
Examples:

•Thermometer – mercury height rises as temperature rises
•Car Speedometer – Needle moves farther right as you accelerate
•Stereo – Volume increases as you turn the knob.

DIGITAL SIGNALS

- A digital signal is a representation of data using a sequence of discrete levels, often binary, where each level corresponds to a specific data value.

- Binary signals operate with two discrete states, typically denoted as 0 (low) and 1 (high).

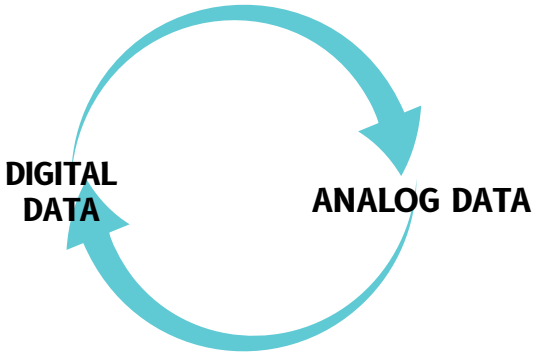


Examples:

•Light switch can be either on or off
•Door to a room is either open or closed

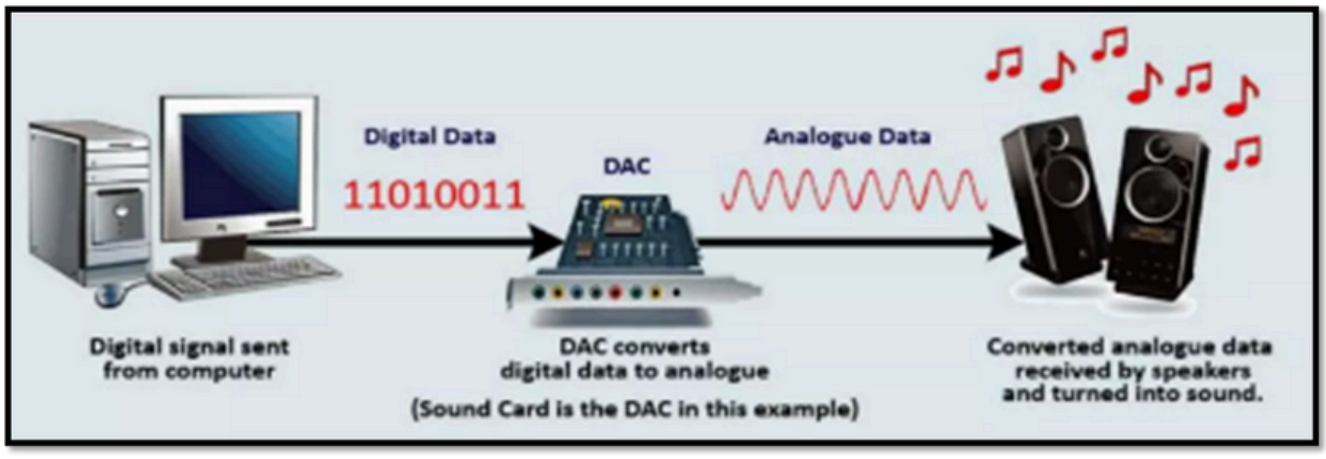
DA CONVERTERS (DAC)

A DAC transforms digital data into analog signals



How It Works

- The DAC receives digital input (usually in binary format).
- It converts this into a corresponding voltage level or current.
- The result is a smooth, continuous waveform that can drive analog devices.



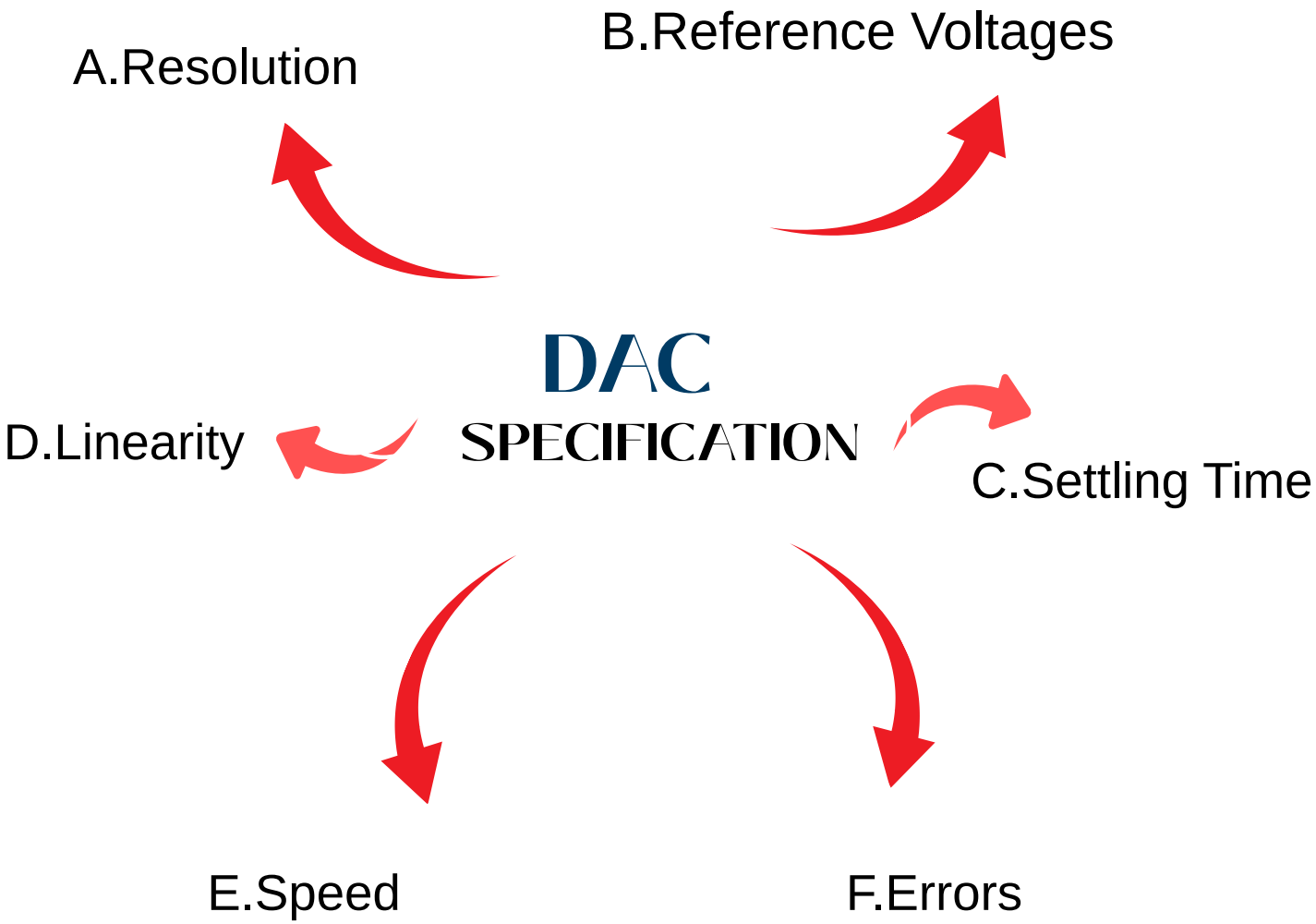
DIGITAL TO ANALOGUE CONVERTERS (DAC)

A Digital-to-Analogue Converter (DAC) is a device that converts a digital input signal (binary) into an analogue signal, such as current, voltage, or electric charge.

Applications:

1.Audio systems in headphones and speakers.
2.Display drivers for analogue screens.
3.Control systems (e.g., motor speed control).
4. Video systems (TVs, display)

SPECIFICATION OF DAC



RESOLUTION

•Resolution is defined as the smallest change in the analogue output that can be produced by a change in the digital input.

•For example, a 10-bit DAC has a higher resolution than an 8-bit DAC. Since it can represent more discrete levels, the smallest change in its output is smaller than that of an 8-bit DAC.

•Resolution is typically expressed either as an absolute value (such as volts or amperes) or as a percentage of the full-scale output range.

•Higher resolution means smaller steps, resulting in a smoother and more accurate analog signal.

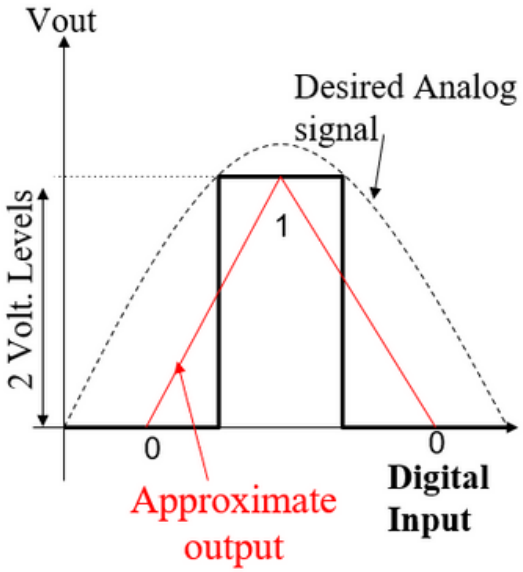
•Lower resolution can lead to a stair-step effect and more distortion, especially in audio or waveform applications.

•A DAC with higher resolution can better represent subtle changes in signal levels.

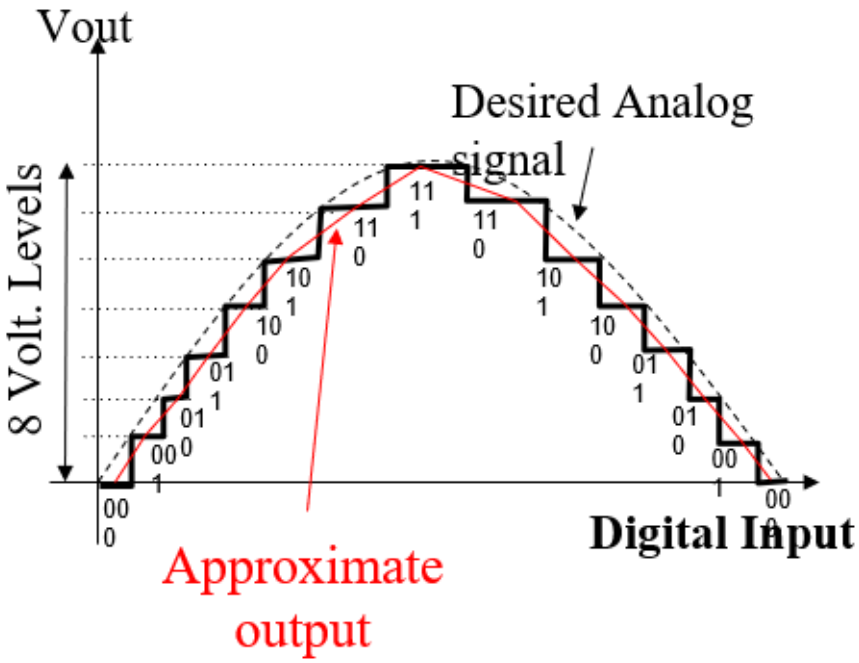
•Common DAC resolutions: 8-bit, 10-bit, 12-bit, 16-bit, even 24-bit for high-fidelity audio

RESOLUTION

POOR RESOLUTION(1 BIT)



BETTER RESOLUTION(3 BIT)



RESOLUTION

Formula:

$$\text{Resolution (in volts)} = \frac{V_{\text{ref}}}{2^n}$$

Where:

- V_{ref} = Reference voltage (maximum output voltage)
- n = Number of bits in the digital input

Example:

For an **8-bit DAC** with a reference voltage of **5V**:

$$\text{Resolution} = \frac{5V}{2^8} = \frac{5V}{256} \approx 0.0195V$$

So, the analog output changes in steps of approximately **19.5 millivolts** for each change in the digital input.

RESOLUTION

Two terms you need to know in resolution are :

1. **step size**
2. **full scale**

STEP SIZE

Step size is the smallest change in the analogue output that corresponds to a one-bit change in the digital input.

Formula:

$$\text{Step Size} = \frac{\text{Full Scale Output Voltage}}{2^n - 1} \quad \text{OR} \quad \text{Step Size} = \frac{V_{\text{ref}}}{2^n - 1}$$

Where:

- n = Number of bits of the DAC
- Full Scale Output = Maximum analog output voltage (usually equal to V_{ref})

RESOLUTION

STEP SIZE

Example:

For an 8-bit DAC with a full-scale output of 5V:

$$\text{Step Size} = \frac{5V}{2^8 - 1} = \frac{5V}{255} \approx 0.0196V$$

So, each step in the output increases by approximately 19.6 mV.

Example:

8-bit DAC with $V_{\text{ref}} = 5V$:

$$\text{Step Size} = \frac{5V}{2^8 - 1} = \frac{5V}{255} \approx 0.0196V$$

So, the analog output increases by ~0.0196V for each step in the digital input.

RESOLUTION

STEP SIZE

Total step and number of step:

For an **n-bit DAC**, the total number of discrete steps is:

$$\text{Total Steps} = 2^n$$

But since the steps start from 0, the number of **output voltage increments** is:

$$\text{Number of Step Increments} = 2^n - 1$$

RESOLUTION

FULL SCALE

Full Scale is the maximum analogue output value that a DAC can produce when all digital input bits are set to 1. Also called Total Step Size.

Formula:

$$\text{Total Step Size} = (2^n - 1) \times \text{Step Size} = V_{\text{ref}}$$

Since the step size is:

$$\frac{V_{\text{ref}}}{2^n - 1}$$

Multiplying it by $(2^n - 1)$ gives back V_{ref}

🔍 Example (continued):

Using the same 8-bit DAC with 5V reference:

- Step size = 0.0196V
- Number of steps = 255
- Total step size =

$$255 \times 0.0196V \approx 5V$$

✅ So, **total step size = full-scale voltage = 5V**

📊 Summary Table

Term	Meaning	Formula	Example (8-bit, 5V)
Step Size	Smallest change in analog output per 1-bit digital input step	$\frac{V_{ref}}{2^n - 1}$	~0.0196 V
Total Step Size	Total analog output range from 0 to full scale	$(2^n - 1) \times \text{Step Size}$	5 V

📊 Quick Summary Table:

Digital Input (Binary)	Decimal Value	Analog Output (Volts)
00000000	0	0 V
00000001	1	0.0196 V
...	...	...
11111111	255	5 V (Full Scale)

RESOLUTION

% RESOLUTION:

n = Number of Bit

$$\% \text{ Resolution} = \frac{1}{2^n - 1} \times 100$$

OR

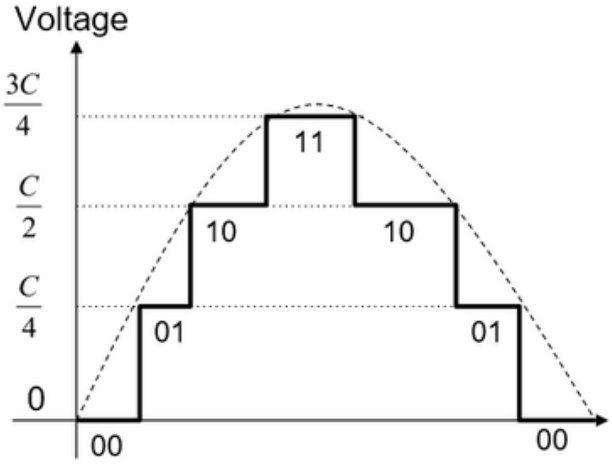
$$\% \text{ Resolution} = \frac{step\ size}{full\ scale\ volatge} \times 100$$

REFERENCE VOLTAGE

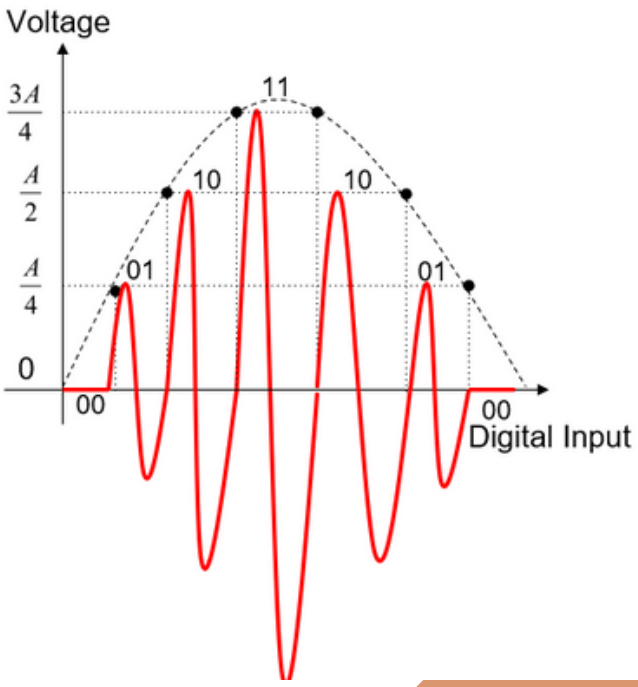
A reference voltage is a specified voltage used to determine how each digital input corresponds to a particular voltage level or range."

Types:
-Non-multiplier: internal, fixed, and defined by manufacturer
-Multiplier: external, variable, user specified

Non-Multiplier: ($V_{ref} = C$)



Multiplier: ($V_{ref} = A\sin(wt)$)



SETTLING TIME

Settling time is the amount of time a system takes to reach and stay within a certain error band (usually a small percentage like ±2% or ±0.1%) of its final value after a change in input, such as a step signal.

In fast systems (like data converters), shorter settling time means faster and more accurate performance.

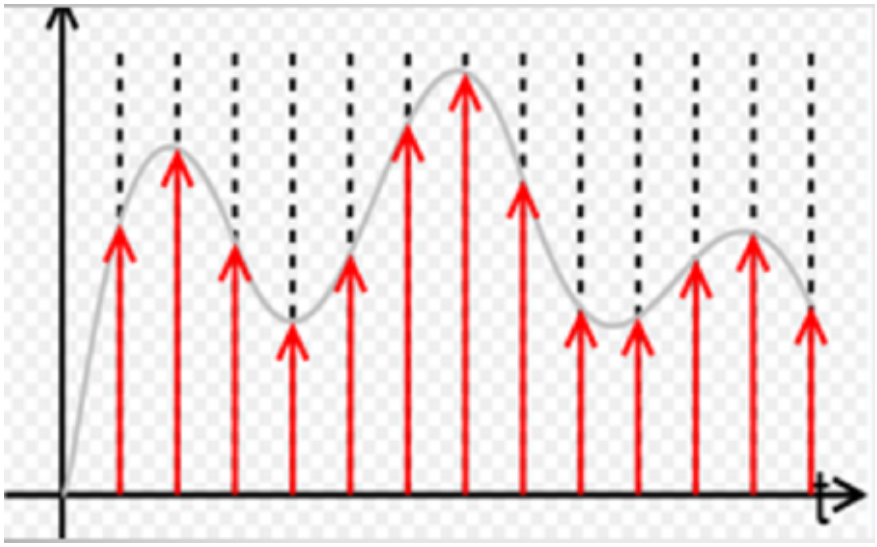
Example:

Suppose a DAC changes its output from 0V to 5V.

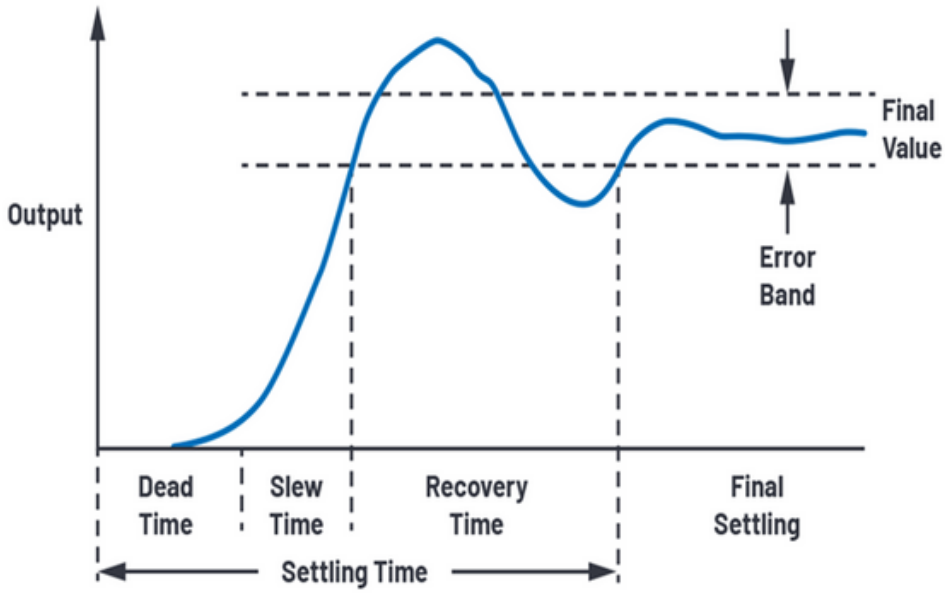
If the output rises quickly to 5V but overshoots to 5.2V, then oscillates and finally settles within **±0.1V** of 5V after **8 microseconds**, then:

> **Settling time = 8 µs (to within ±2%)**

SETTLING TIME



Ideal DAC

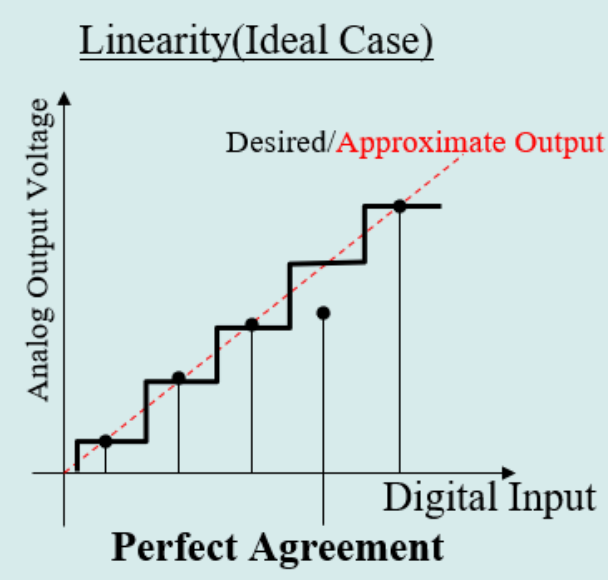


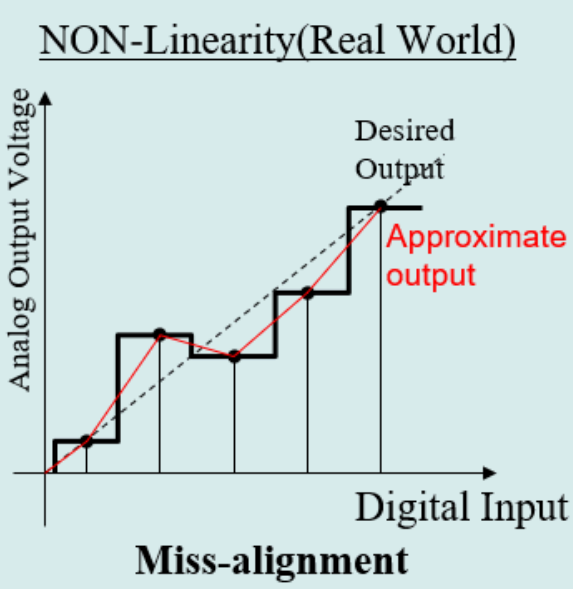
Real DAC

•Ideally a DAC would instantaneously change its output value when the digital input would change.
•In a real DAC it takes time for the DAC to reach the actual expected output value.

LINEARITY

- Linearity in electronics and systems refers to how accurately the output of a device or system follows a straight-line relationship with its input.
- Non-linearity causes distortion and error in measurements or signal conversion.



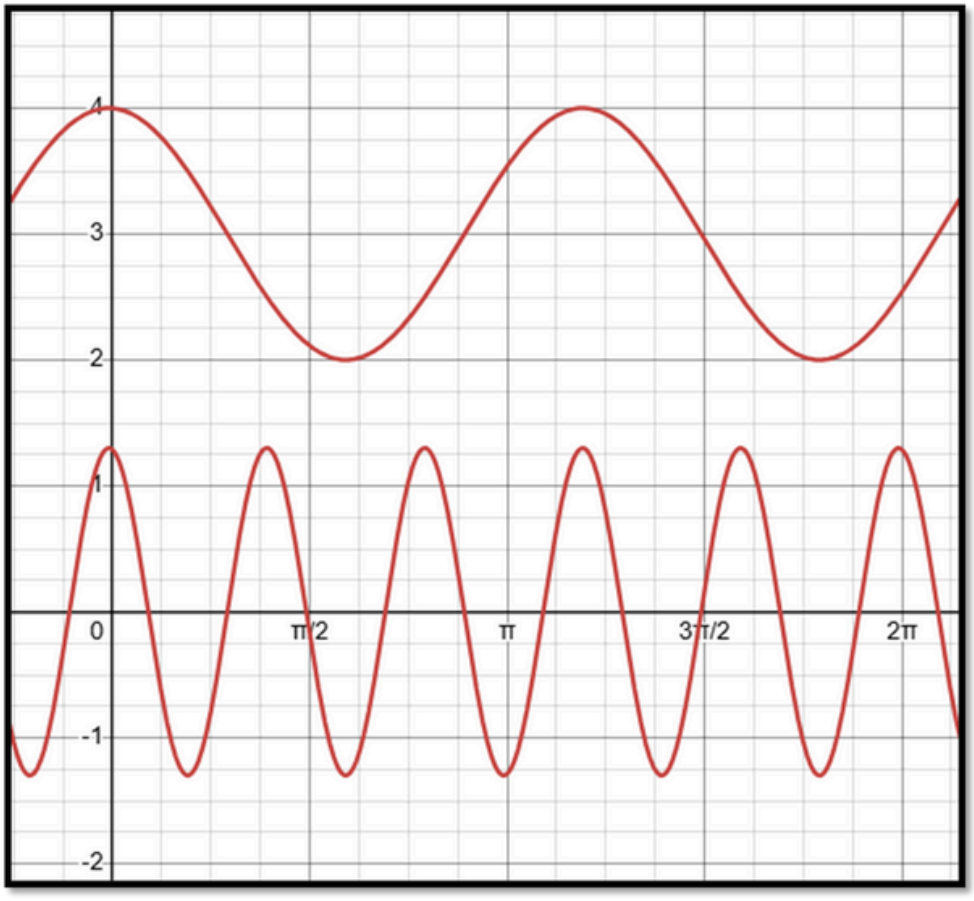


SPEED

What?

In electronics, speed refers to how fast a device or system responds, processes, or transfers data. It's a key performance metric for components like ADC, DAC.

Determines how rapidly a DAC can translate digital values into analog voltages.



ERROR

•Error is the difference between the actual (measured or output) value and the ideal or expected value. It tells you how accurate or inaccurate a system is.

•A DAC error occurs when the analogue output does not exactly match the expected value for a given digital input. These errors reduce accuracy and linearity.

•Non-linearity
-Differential
-Integral

•Gain

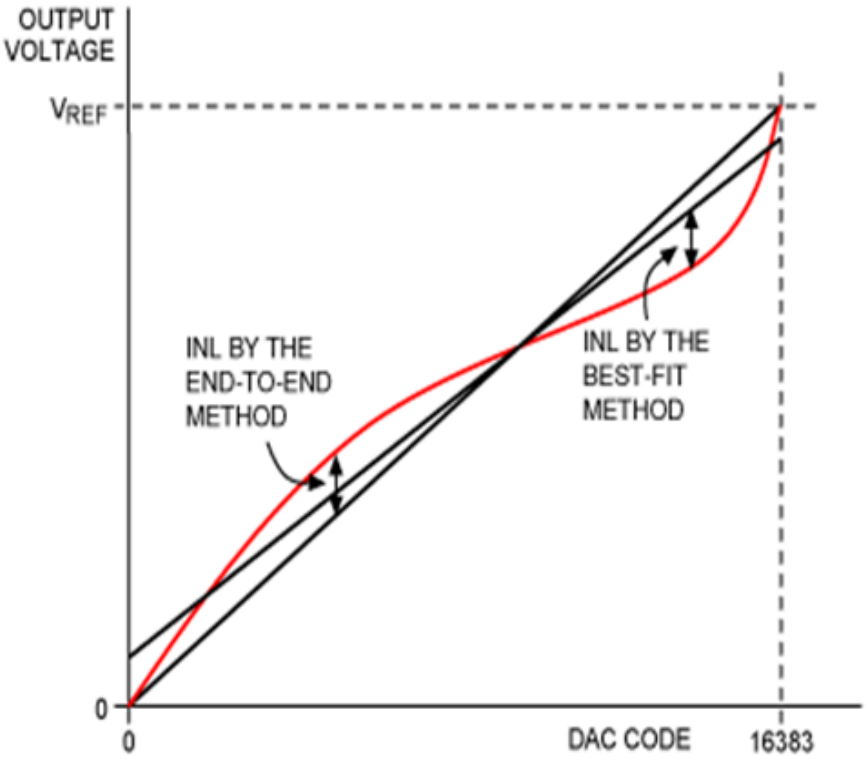
•Offset

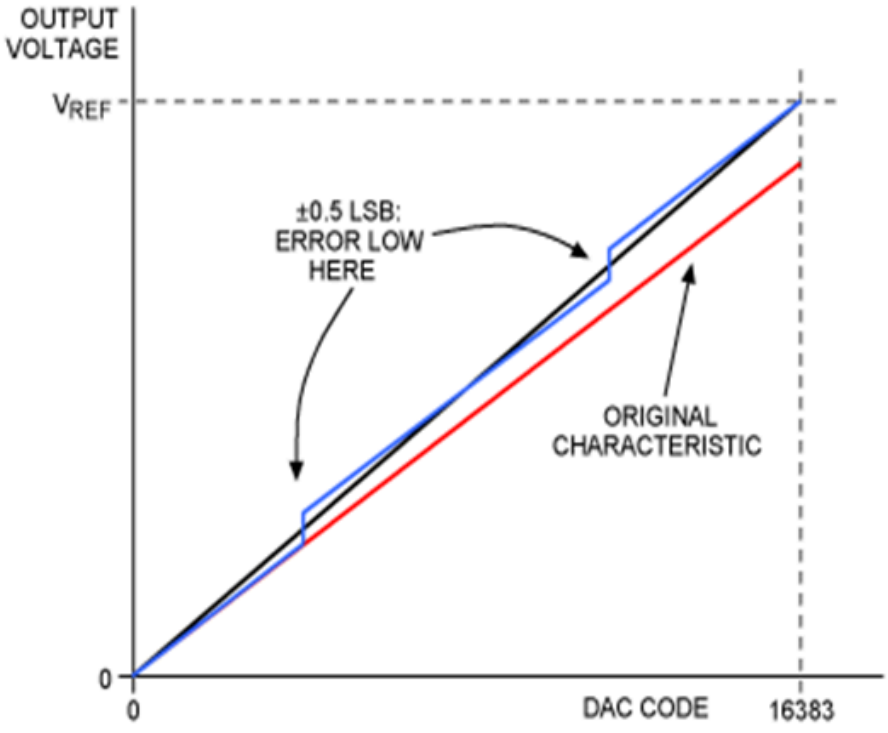
•Non-monotonicity

🔍 Common Types of DAC Errors:

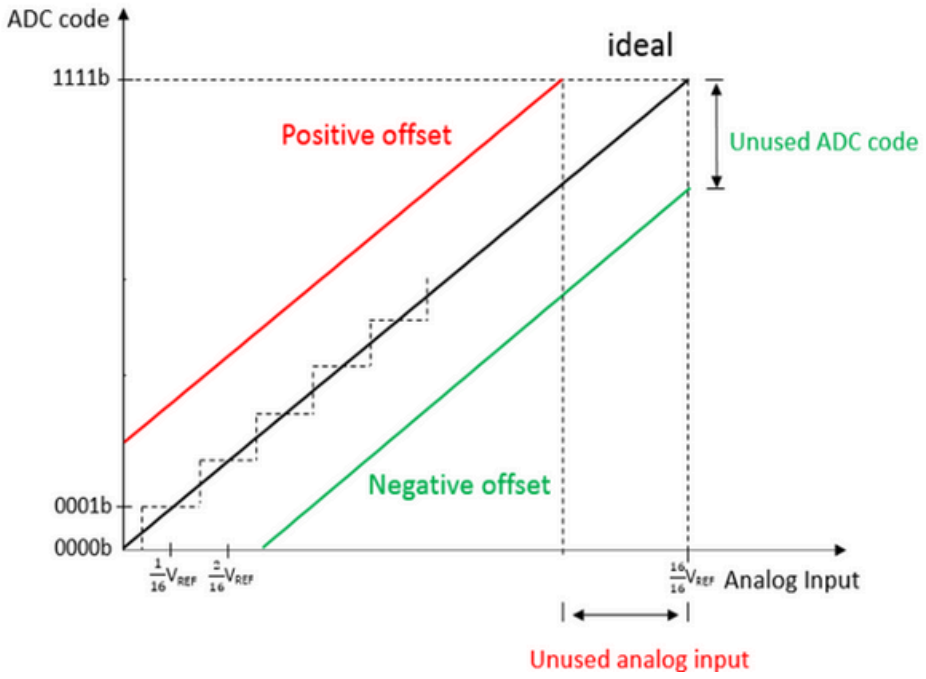
Type of Error	Description	Example
Offset Error	Output is shifted up or down by a constant voltage	All outputs are +0.05V too high
Gain Error	Output slope is incorrect, often due to reference voltage mismatch	Final value is slightly too high or low
Differential Non-Linearity (DNL)	Difference between steps is not uniform	One step is larger or smaller than expected
Integral Non-Linearity (INL)	Deviation of actual output from the ideal straight-line curve	Output curve bends instead of staying linear

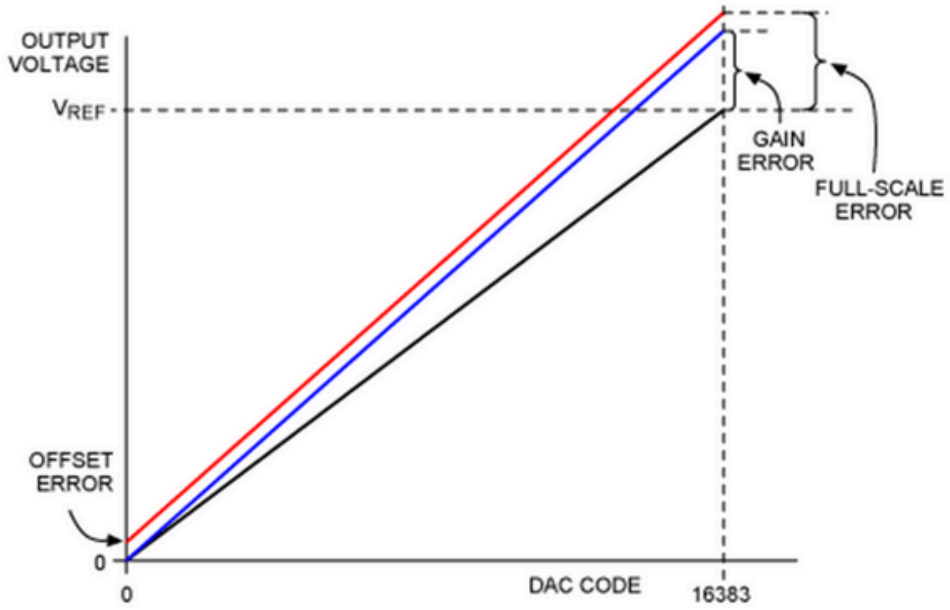
ERROR


OUTPUT VOLTAGE
VREF
INL BY THE END-TO-END METHOD
INL BY THE BEST-FIT METHOD
0
0
DAC CODE
16383

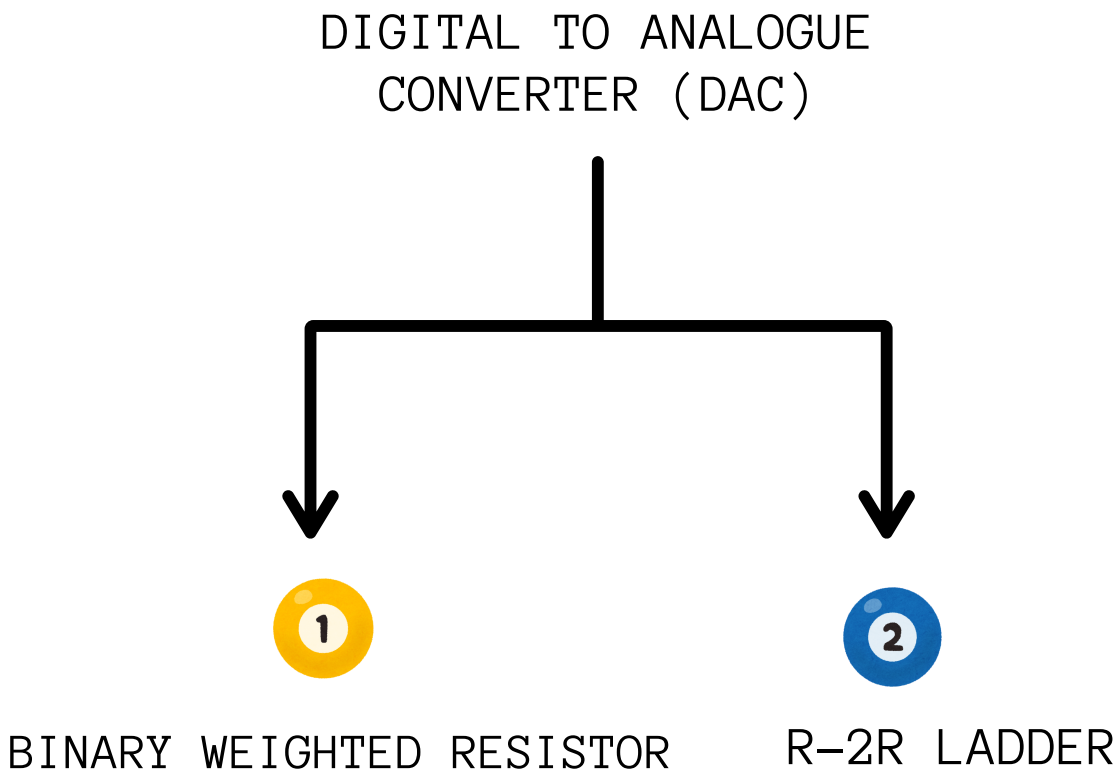

OUTPUT VOLTAGE
VREF
±0.5 LSB: ERROR LOW HERE
ORIGINAL CHARACTERISTIC
0
0
DAC CODE
16383

ERROR

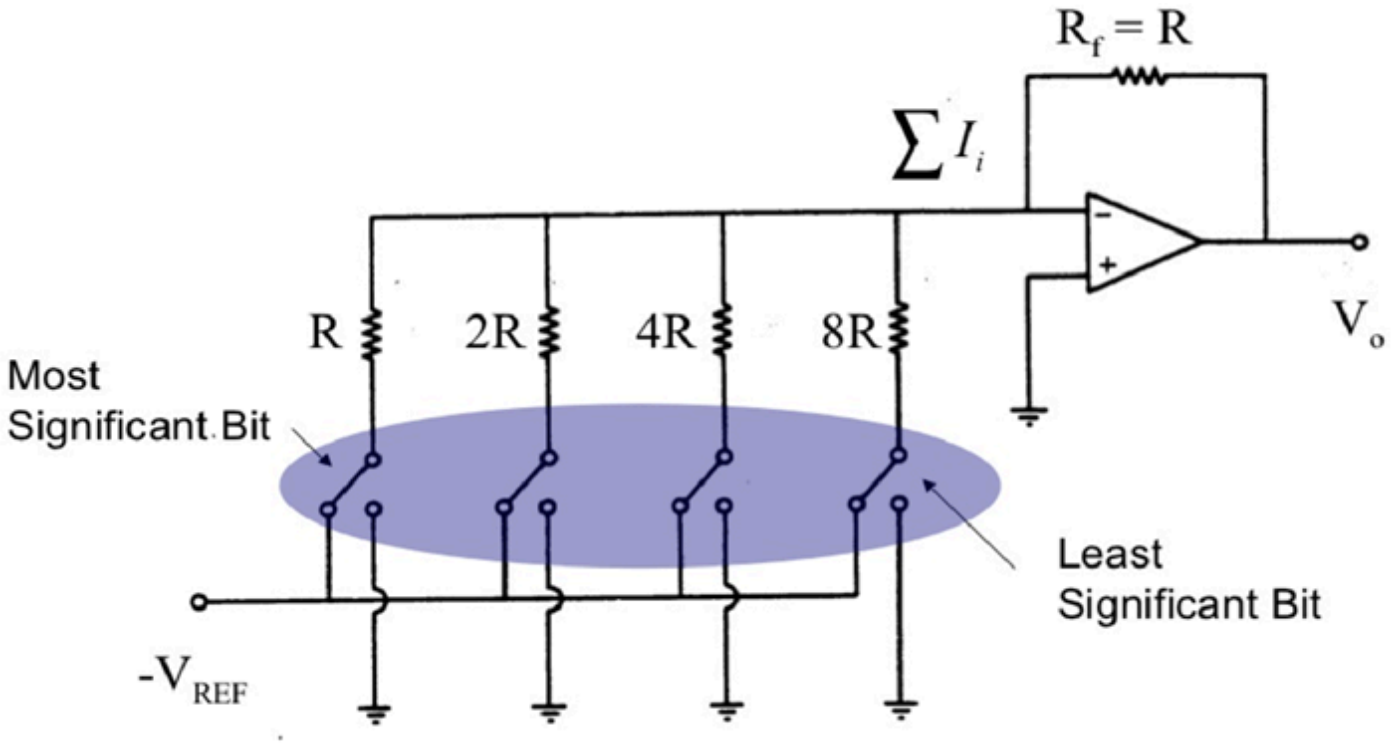

ADC code
ideal
1111b
Positive offset
Unused ADC code
Negative offset
0001b
0000b
Analog Input
Unused analog input


OUTPUT VOLTAGE
VREF
GAIN ERROR
FULL-SCALE ERROR
OFFSET ERROR
0
0
DAC CODE
16383

DIGITAL TO ANALOGUE CONVERTER TYPES

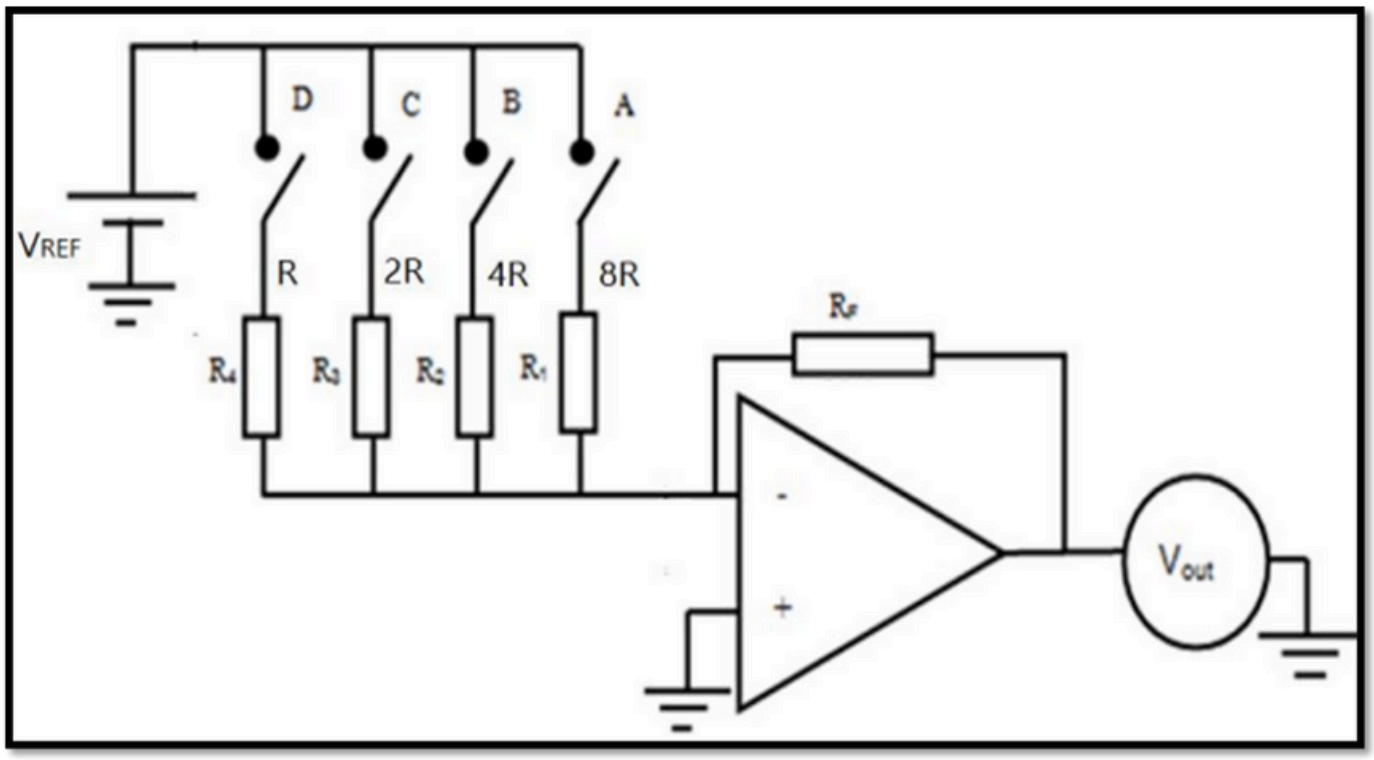


BINARY WEIGHTED RESISTOR



A binary-weighted resistor digital-to-analogue converter (DAC) converts a digital input signal into an equivalent analogue output using a network of resistors weighted according to binary values.

BINARY WEIGHTED RESISTOR



•The resistor values are weighted based on binary place value (R, 2R, 4R, 8R, etc.). MSB (Most Significant Bit) controls the smallest resistor (R), LSB (Least Significant Bit) controls the largest resistor (8R in 4-bit DAC).

•All resistors connect into an op-amp summing amplifier to produce an analogue output.

1ST EQUATIONS

$$\sum I = V_{REF}\left(\frac{B_3}{R}+\frac{B_2}{2R}+\frac{B_1}{4R}+\frac{B_0}{8R}\right)$$

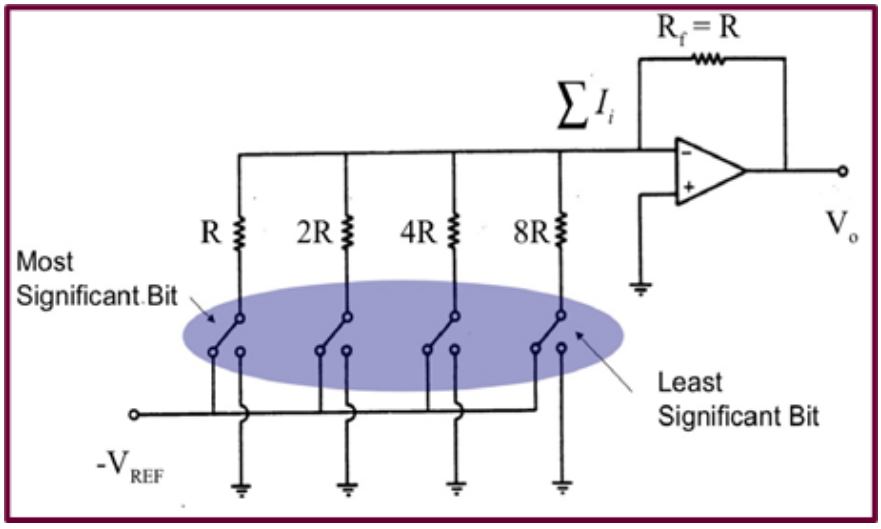
$$V_{OUT} = I \cdot R_f = V_{REF}\left(B_3+\frac{B_2}{2}+\frac{B_1}{4}+\frac{B_0}{8}\right)$$

B_i = Value of Bit i

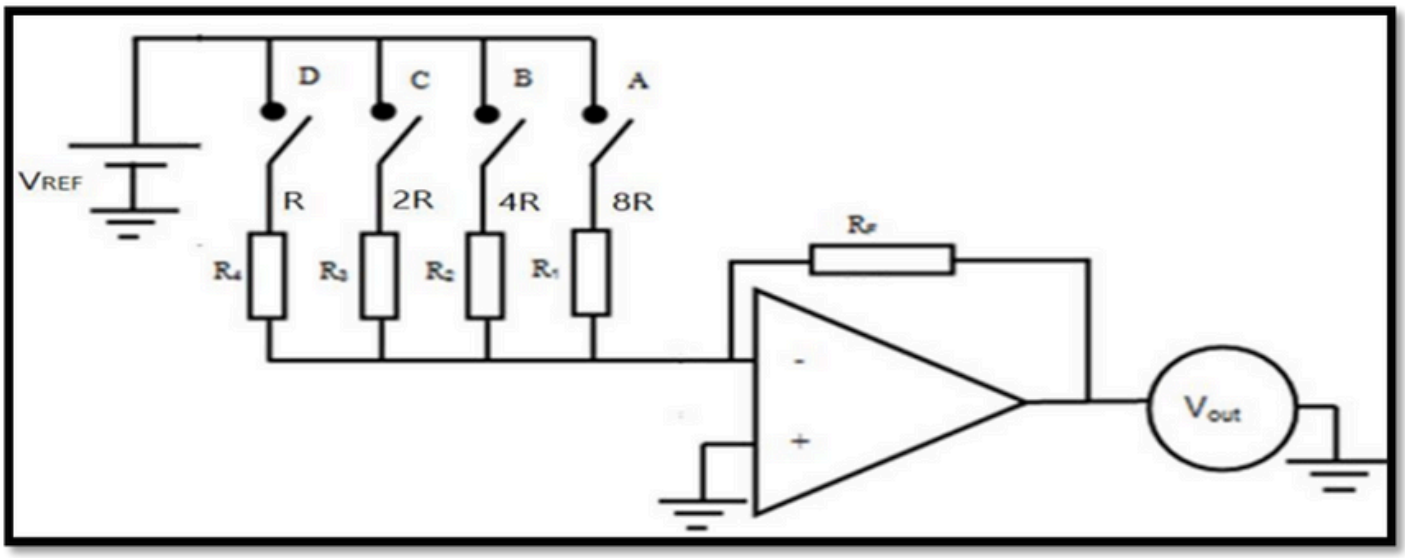
$$V_{OUT} = V_{REF}\sum\frac{B_i}{2^{n-i-1}}$$

$$= V_{REF} \cdot \text{Digital Value} \cdot \text{Resolution}$$

- B_i = Value of Bit i
- n = Number of Bits



1ST EQUATIONS



$$V_{out} = -R_F\left(\frac{D}{R} + \frac{C}{2R} + \frac{B}{4R} + \frac{A}{8R}\right) \bullet V_{REF}$$

Example : Calculate Vout for digital input 1011

$$V_{out} = -10k\left(\frac{1}{25k} + \frac{0}{50k} + \frac{1}{100k} + \frac{1}{200k}\right) \bullet 5 \Longrightarrow V_{out} = 2.75V$$

2ND EQUATIONS

$$V_{out} = V_{ref} \times A_V$$

$$Vout = Vref\left(\frac{Rf}{R1} + \frac{Rf}{R2} + \frac{Rf}{R3} + \frac{Rf}{R4}\right)$$

$$Av = \sum \frac{Rf}{Ri}$$

Ri = R1, R2, R3, R4

EXAMPLE

$$Voltage\,Gain, A_V = -\Sigma \frac{R_F}{R_i}$$

$$V_{OUT} = V_{REF}\, x\, A_V$$

Example:

R_1 = 200K, R_2 = 100K, R_3 = 50K, R_4 = 25K, R_F = 10K, V_{REF} = 5V,

Vout for a number of digital inputs, binary Input = 1011.

$$Voltage\,Gain, A_V = -\Sigma \frac{R_F}{R_i}$$

$$A_v = -\left[\frac{10k}{25k} + \frac{10k}{100k} + \frac{10k}{200k}\right]$$

$$A_v = -[0.4 + 0.1 + 0.05]$$

$$A_v = -0.55$$

$$V_{OUT} = V_{REF}\, x\, A_V$$

$$V_{OUT} = 5(-0.55)$$

$$V_{OUT} = 2.75V$$

Vout for a number of digital inputs:

- **Binary Input = 1111** *(4 resistor involve)*

  R_1 = 200K R_2 = 100K R_3 = 50K R_4 = 25K

  R_F = 10K

  ∴ voltage gain (A_V) = $\Sigma \frac{R_f}{R_i} = \frac{10K}{25K} + \frac{10K}{50K} + \frac{10K}{100K} + \frac{10K}{200K}$

  = (0.4 +0.2+0.1+0.05) = 0.75

$V_{out} = V_{ref}$ X A_V = 5 X 0.75 = 3.75V

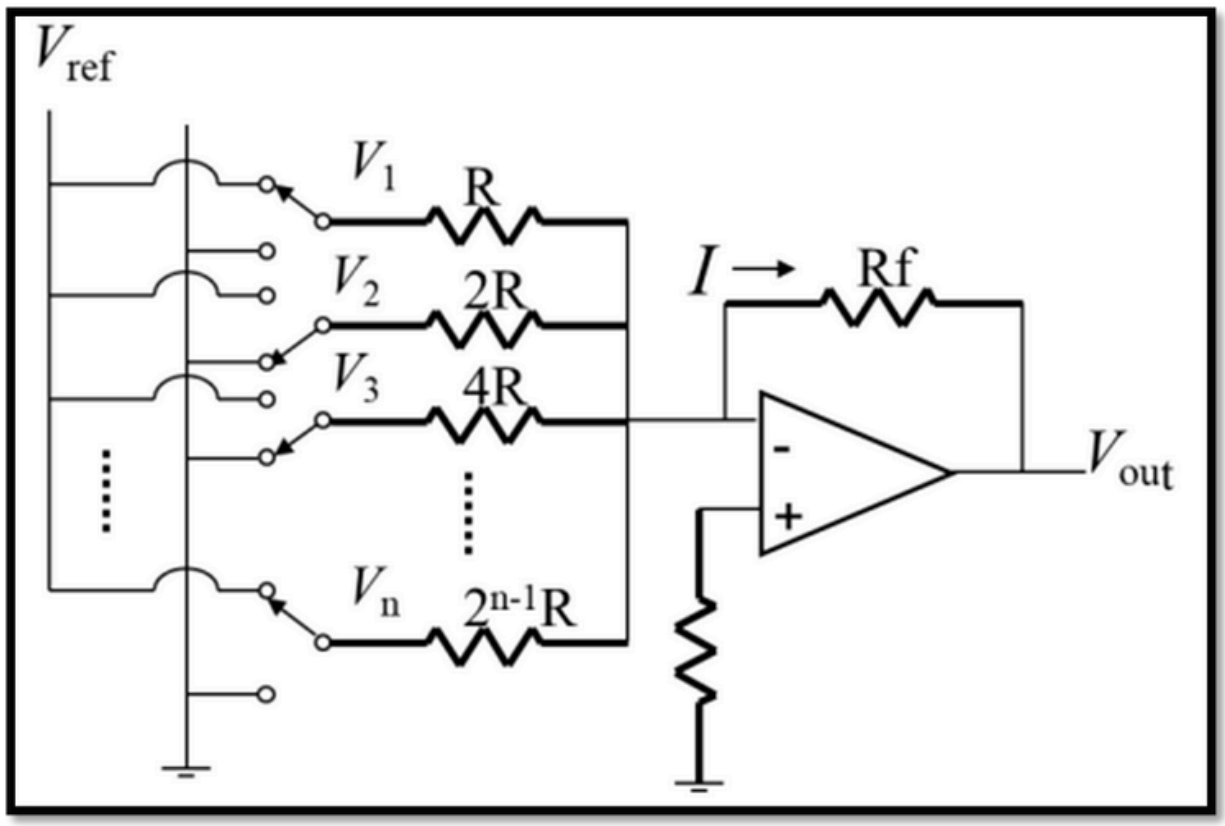
3RD EQUATIONS

$$V_{out} = -IR_f$$

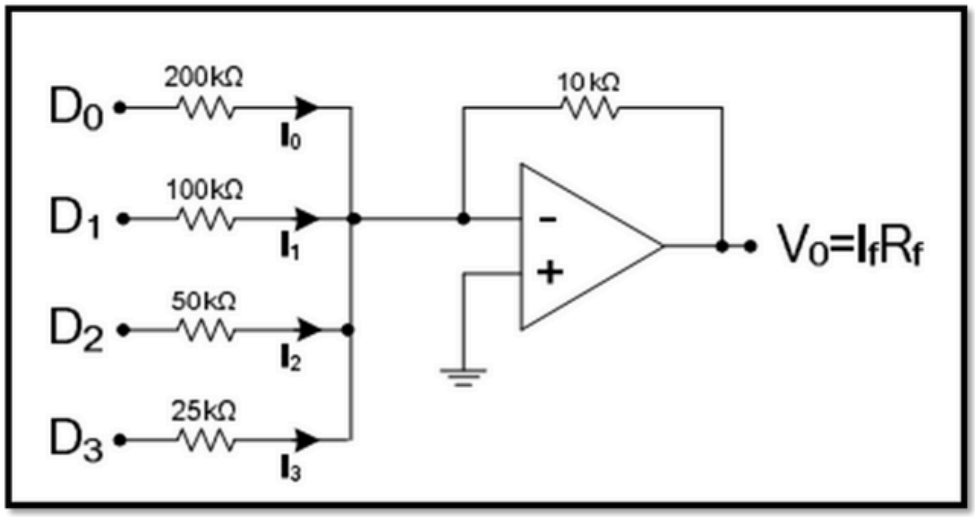
$$V_{out} = -IR_f = -R_f\left(\frac{V_1}{R} + \frac{V_2}{2R} + \frac{V_3}{4R} + \cdots \frac{V_n}{2^{n-1}R}\right)$$

MSB

LSB



EXAMPLE



For a +5V input (Vref), the current at each input are:

$$I_0 = \frac{V_{ref}}{R_1} = \frac{5V}{200K} = 0.025mA$$

$$I_1 = \frac{V_{ref}}{R_2} = \frac{5V}{100K} = 0.05mA$$

$$I_2 = \frac{V_{ref}}{R_3} = \frac{5V}{50K} = 0.1mA$$

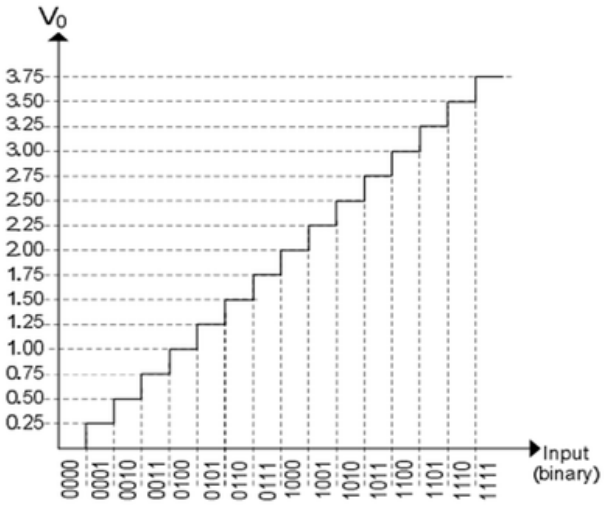
$$I_3 = \frac{V_{ref}}{R_4} = \frac{5V}{25K} = 0.2mA$$

Therefore,

Vout = Rref x I,

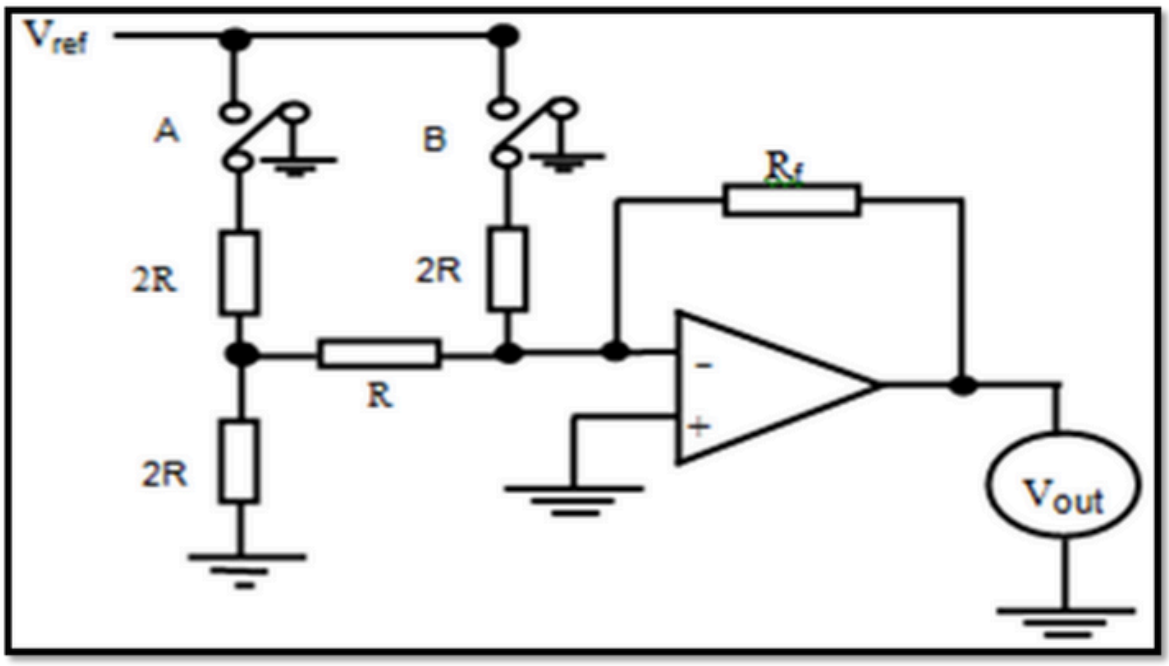
- $V_{out(D0)}$ = 10kΩ x 0.025mA = 0.25V
- $V_{out(D1)}$ = 10kΩ x 0.05mA = 0.5V
- $V_{out(D2)}$ = 10kΩ x 0.1mA = 1V
- $V_{out(D3)}$ = 10kΩ x 0.2mA = 2V

Decimal	Input binary				V_{out} (V)
	D3	D2	D1	D0	
0	0	0	0	0	0
1	0	0	0	1	0.25
2	0	0	1	0	0.50
3	0	0	1	1	0.75
4	0	1	0	0	1.00
5	0	1	0	1	1.25
6	0	1	1	0	1.50
7	0	1	1	1	1.75
8	1	0	0	0	2.00
9	1	0	0	1	2.25
10	1	0	1	0	2.50
11	1	0	1	1	2.75
12	1	1	0	0	3.00
13	1	1	0	1	3.25
14	1	1	1	0	3.50
15	**1**	**1**	**1**	**1**	**3.75**



R–2R LADDER

1. The R-2R ladder forms a voltage divider network using only resistors of value R and 2R.
2. Switch A is the LSB input switches and switch B is switch the input MSB.



Then the general expression for the circuit is

$$V_{out} = \frac{V_{ref}}{2^n} \times B_{in} \times \frac{R_f}{R}$$

where :

n = number of bits

Bin = digital input converted to decimal numbers

Full scale output of the 2 bit R-2R Ladder circuit is by setting the input will produce binary bit 11 = Vout = Vref.

R–2R LADDER

- Input $01_2 = 1_{10}$, Vout = $\frac{V_{ref}}{4}\frac{R_f}{R}$
- Input $10_2 = 2_{10}$, Vout = $\frac{V_{ref}}{2}\frac{R_f}{R}$
- Input $11_2 = 3_{10}$, Vout = $\frac{3V_{ref}}{4}\frac{R_f}{R}$

We can get the general equation for output as;

- $V_{0ut} = V_{00} + V_{01} + V_{10} + V_{11} = 0 + \frac{V_{ref}}{4}\frac{R_f}{R} + \frac{V_{ref}}{2}\frac{R_f}{R} + \frac{3V_{ref}}{4}\frac{R_f}{R}$

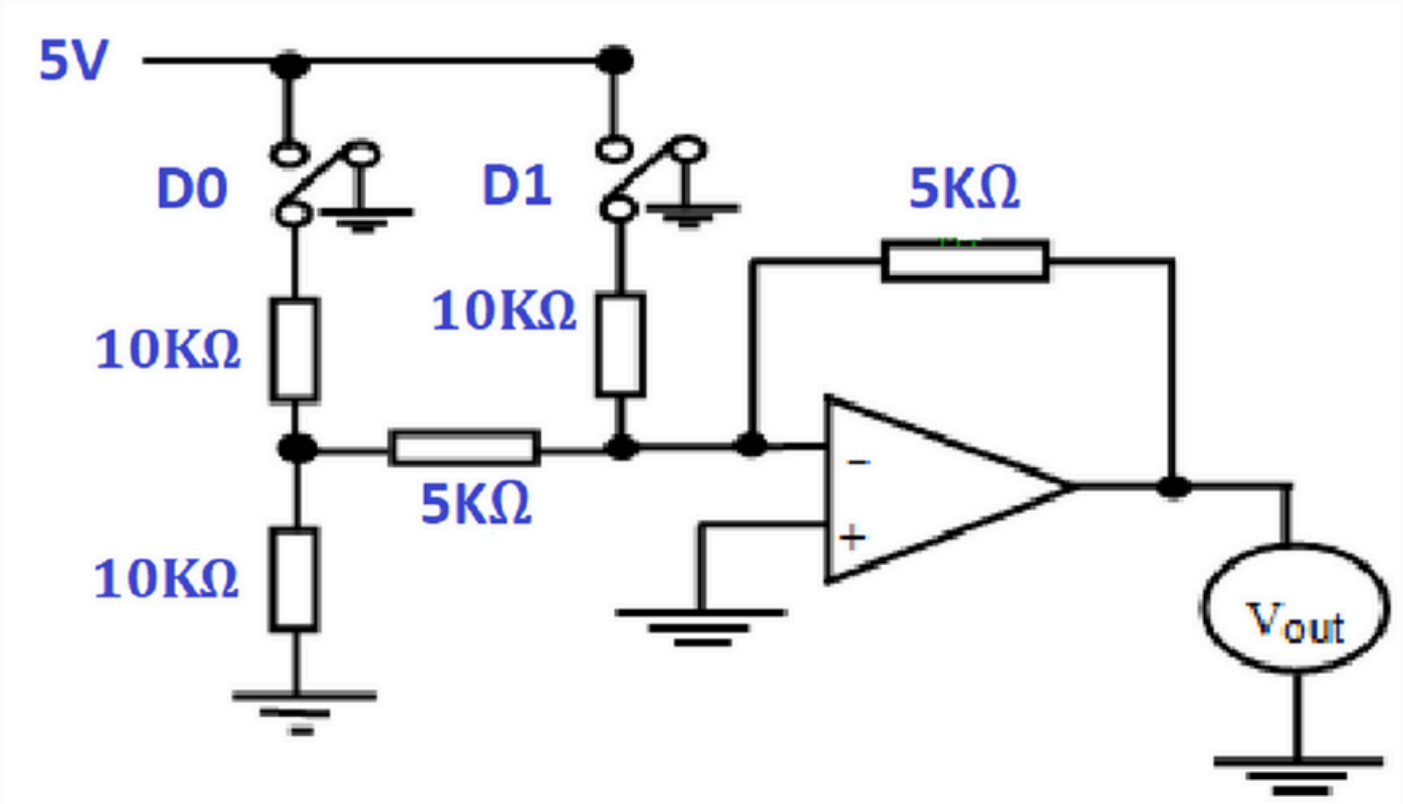
$$\therefore V_{0ut} = \frac{V_{ref}}{4}\frac{R_f}{R}[0+1+2+3]$$

- $\mathbf{V_{out} = \frac{V_{ref}}{2^n}\frac{R_f}{R}B_{in}}$

n = number of bits

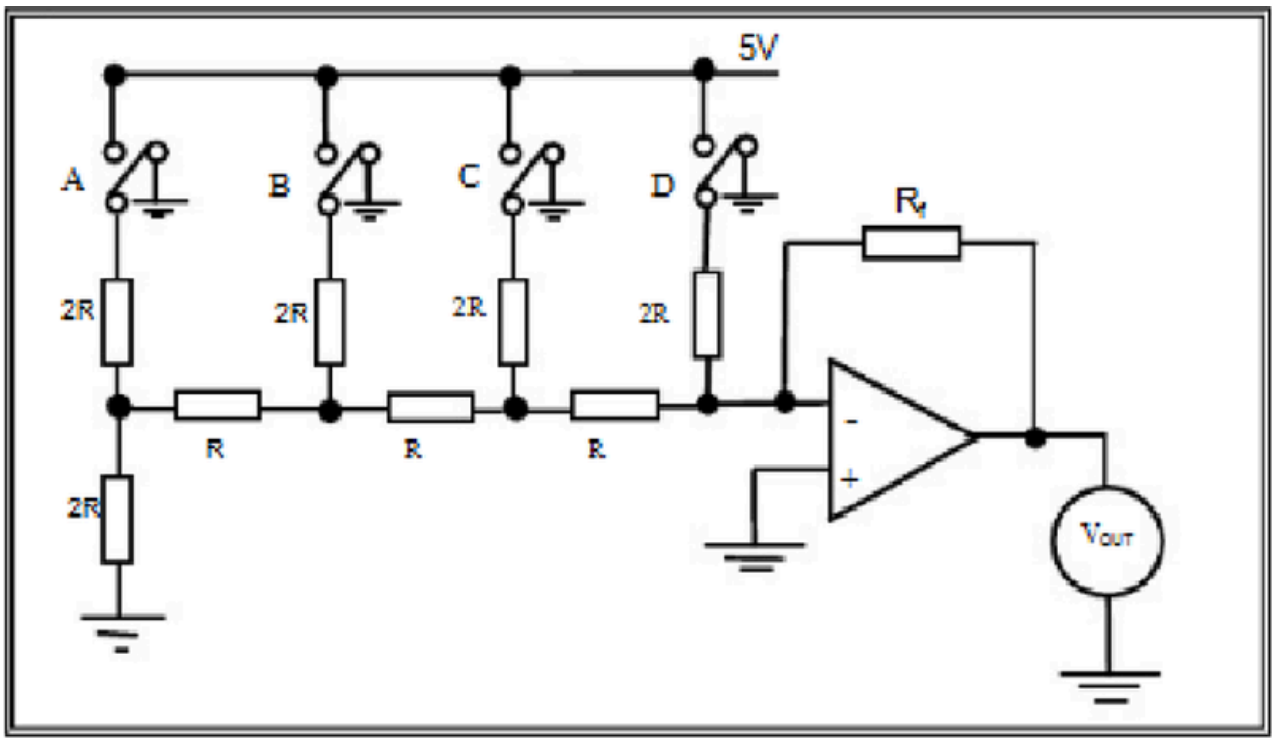
B_{in} = binary input that has been converted to decimal

2 BIT R–2R LADDER CIRCUIT



DECIMAL VALUE	B	A	ANALOGUE VALUE
0	0	0	0
1	0	1	1.25
2	1	0	2.5
3	1	1	3.75

4 BIT R–2R LADDER CIRCUIT



Input				Output, $V_{OUT} = \frac{V_{ref}}{2^n}\frac{R_f}{R}B_{in}$
D	C	B	A	$V_{out} = \frac{5}{2^4}\frac{R}{R}B_{in} = \frac{5}{16}B_{in}$
0	0	0	0	0
0	0	0	1	0.3125
0	0	1	0	0.6250
0	0	1	1	0.9375
0	1	0	0	1.2500
0	1	0	1	1.5625
0	1	1	0	1.8750
0	1	1	1	2.1875
1	0	0	0	2.5000
1	0	0	1	2.8125
1	0	1	0	3.1250
1	0	1	1	3.4375
1	1	0	0	3.75
1	1	0	1	4.0625
1	1	1	0	4.375
1	1	1	1	4.6875

ASSUME RESISTER SAME VALUE RF = R = 1

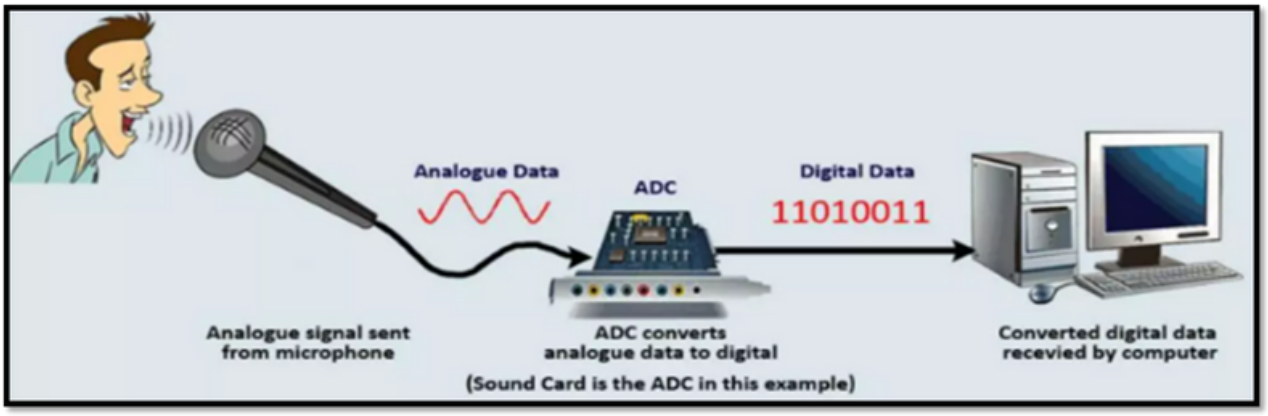
DAC – ADVANTAGES AND DISADVANTAGES

	Binary Weighted	R-2R
Pros	•Simple Analysis. •Fast Conversion. •Easily understood.	•Only Two Resistor Values (R & 2R). •Does Not Require High Precision Resistors. •Easier implementation. •Easier to manufacture. •Faster response time.
Cons	•Requires a wide range of accurate valuess of resistor (10 bit DAC needs resistor ranging from R to R/1024). •Limited to ~ 8 bits resolution. •Susceptible to noise. •Expensive. •Greater Error.	•Lower Conversion Speed. •More confusing analysis.

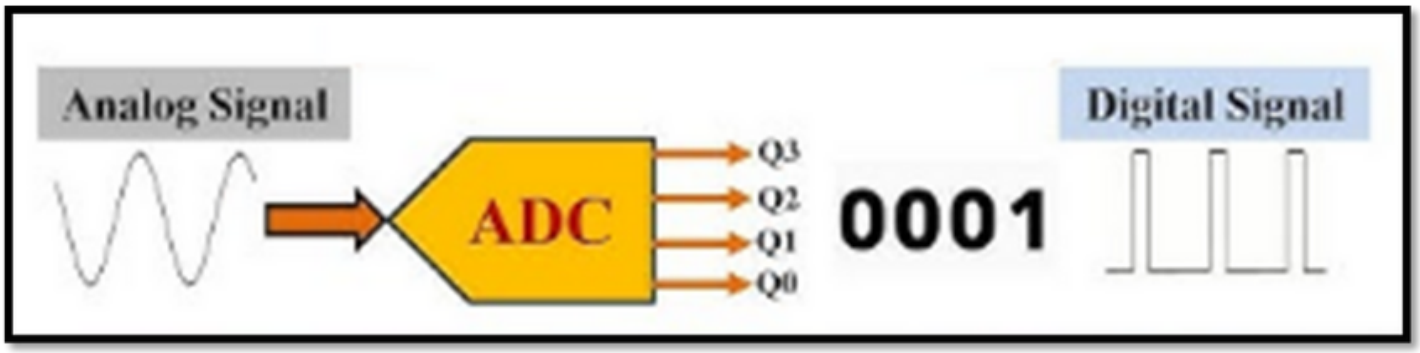
DIFFERENCES BETWEEN BINARY WEIGHTED RESISTOR AND R/2R LADDER

Binary Weighted Binary	R-2R Ladder
1.Simple construction circuit. 2.Use various resister value at each stage . 3.Fast conversion. 4.Easily understood.	1.Slightly complicated circuit. 2.Use two resistor values R & 2R. 3.Complicated to convert. 4.Easier implementation.

ANALOGUE TO DIGITAL CONVERTERS (ADC)



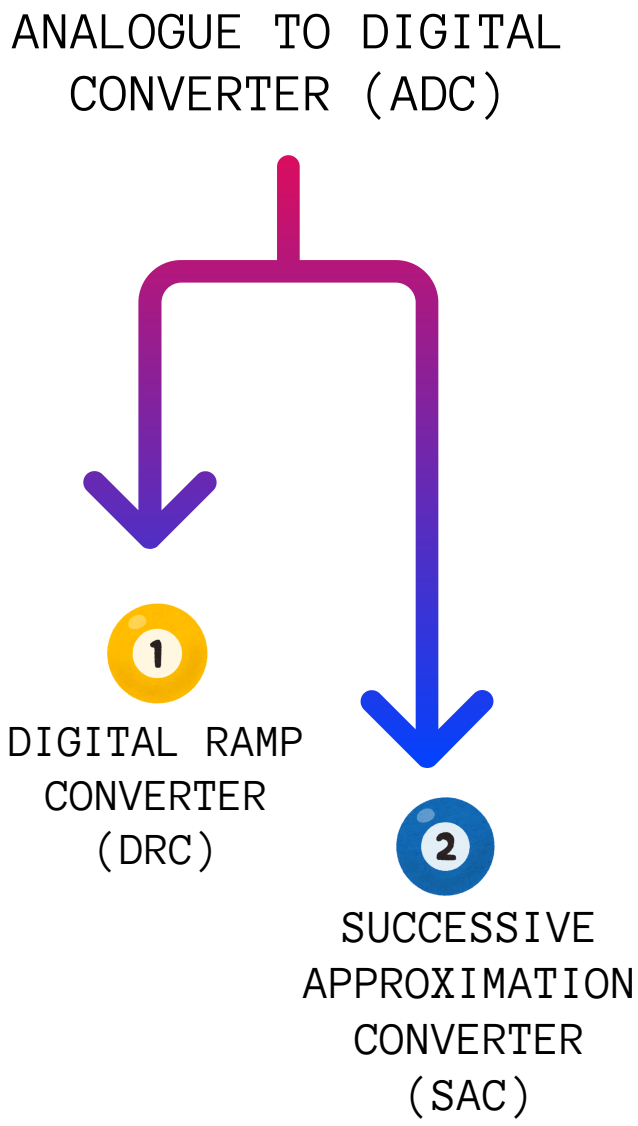
An ADC (Analogue-to-Digital Converter) is an electronic device that converts continuous analogue signals (like sound, temperature, or voltage) into digital binary values that can be processed by digital systems (e.g., microcontrollers, computers).



Applications:

1.Audio recording and playback (microphones, sound cards).
2.Sensors (temperature, light, pressure).
3.Medical devices (ECG, imaging).
4.Robotics, control systems, communication.

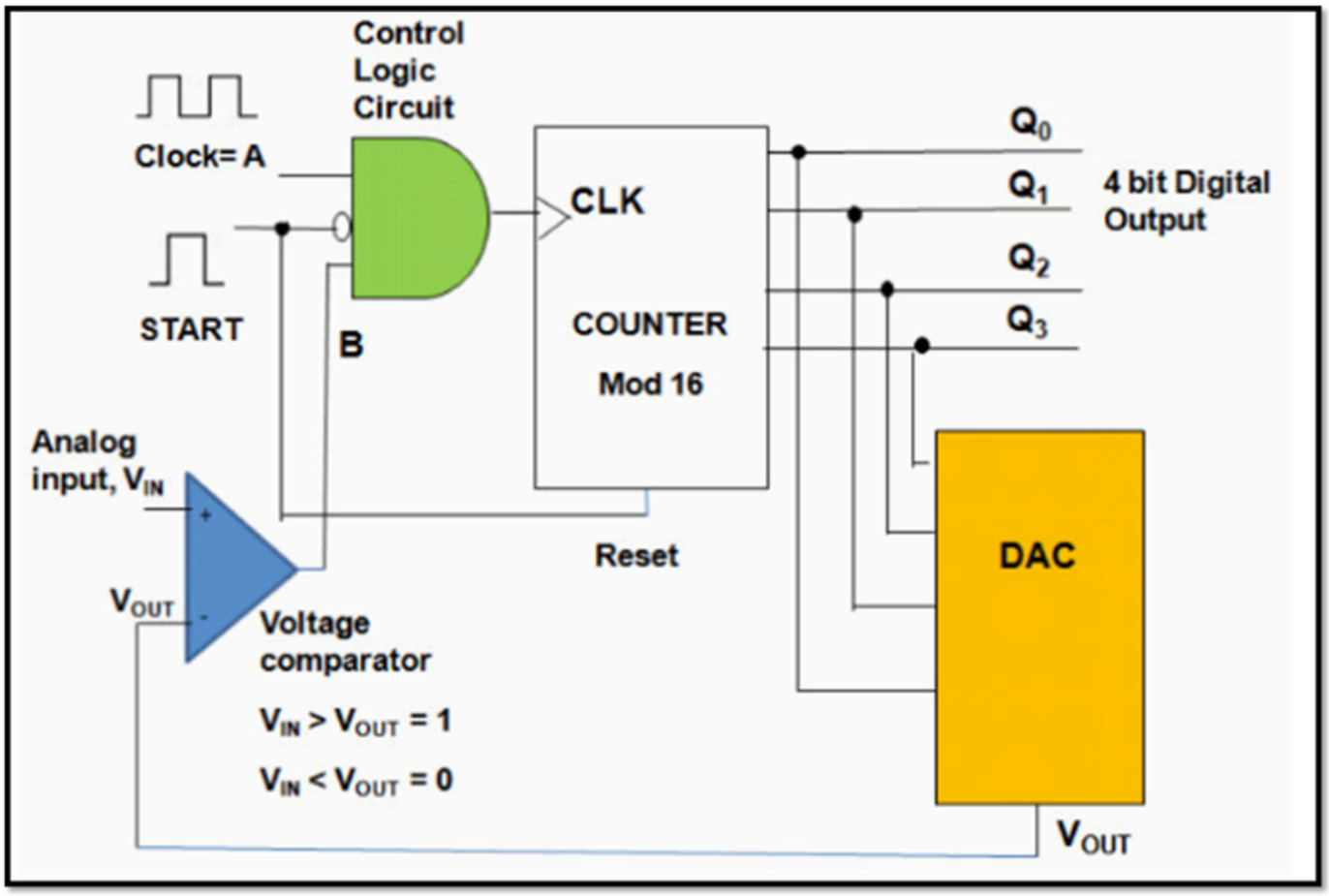
ANALOGUE TO DIGITAL CONVERTER TYPES



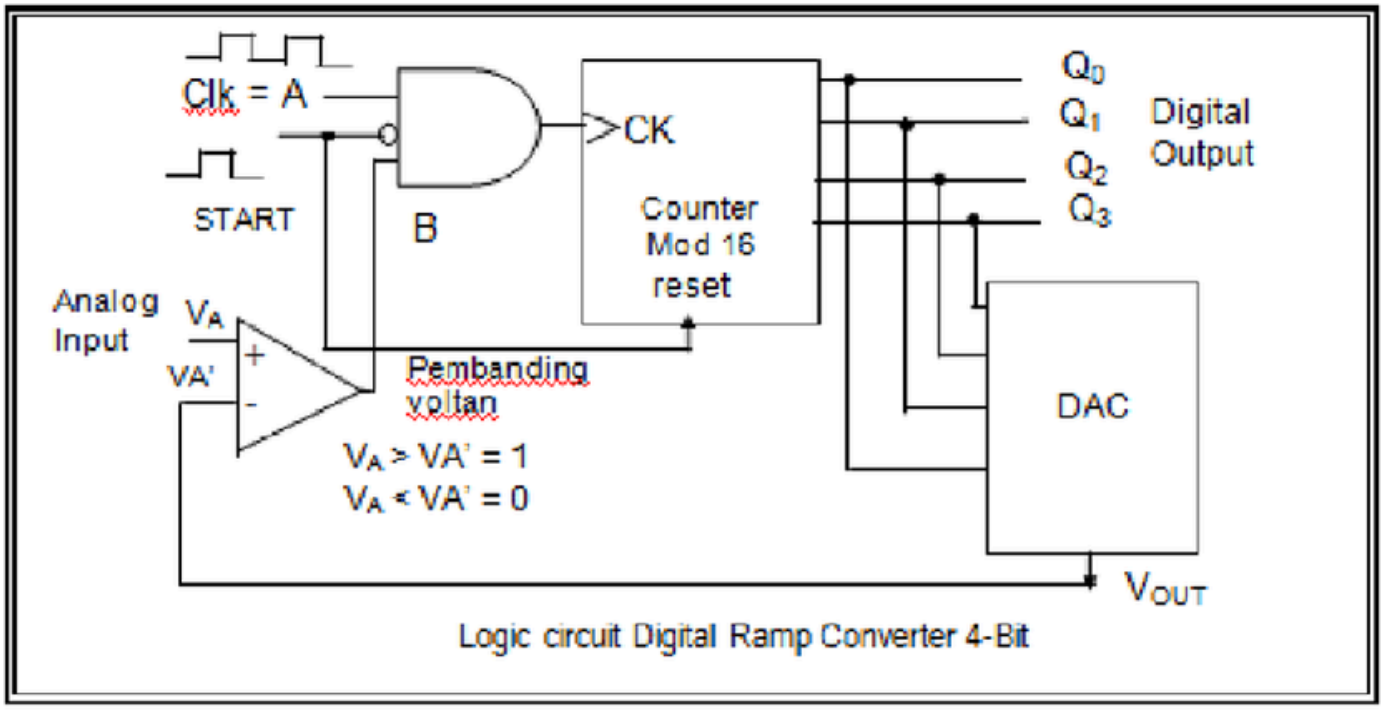
DIGITAL RAMP CONVERTER (DRC)

- A Digital Ramp Converter (DRC), also known as a counter-type ADC, It counting up in binary until the output of a DAC matches the input analog voltage.
- DRC consists of a voltage comparator, logic control, 4-bit counter circuits and digital to analog converter (DAC).
- Voltage comparator is used to compare the analog input voltage and the output voltage from the DAC.
- Control logic circuit used to reset count, when the input is 'START' is given logic high.
- –Counter circuit is used to allow the clock to add a step by step until the output DAC (VA ') greater than or equal to the input analog (VA).

DRC CIRCUIT


Control
Logic
Circuit
Clock= A
START
B
CLK
COUNTER
Mod 16
Q_0
Q_1
Q_2
Q_3
4 bit Digital
Output
Analog
input, V_{IN}
V_{OUT}
Voltage
comparator
$V_{IN} > V_{OUT} = 1$
$V_{IN} < V_{OUT} = 0$
Reset
DAC
V_{OUT}

DRC CIRCUIT OPERATION



Logic circuit Digital Ramp Converter 4-Bit

If the VA is positive, the operation of the circuit is as follows; (assume VA = 5V)

1. A positive 'start' pulse is supplied, and the counters are reset to zero. The AND gate output is low, so the counter does not receive any triggered bell-shaped pulses.
2. When the count at zero, VA '= 0, so the output of the comparator is HIGH because (VA > VA'). When a falling-edge (lower back) triggered pulse occurs, the AND gate output becomes HIGH (since all inputs are at logic HIGH), allowing the counter to begin.
3. The output of the DAC, VA' increases in voltage steps corresponding to the step size or resolution (VA' increased 1v, 2v, 3v, 4v, 5v).
4. This process continues until the VA' ≥ VA (5v ≥ 5v). At that point, the comparator output goes LOW, and the counter stops at the count corresponding to VA. The conversion process is COMPLETE, and the digital output of the DRC is 0101.

DRC CIRCUIT OPERATION

Specifications Digital Ramp Converter

Resolution and accuracy

- same as the resolution and accuracy of the digital to analog converter.

Tc, Conversion Time

- is the time taken to convert the analog input of a digital exit.
- For the digital ramp converters, counters count from 0 to VA' ≥ VA.
- The time for completion of the conversion process, depending on the value of analog input, VA. The greater the value of VA then more steps and longer conversion time.

$$T_{cmax} = (2^n - 1) \text{ X } (1 \text{ clock cycle})$$
$$= (2^n - 1) \text{ x } T_{in}$$
$$= \text{total step x } T_{in}$$

Tcmax, the maximum conversion time occurs when VA ≥ VFS

EXAMPLE 4-BIT DRC

Assumptions for Example:

- Vref = 5V (Full scale voltage)
- Resolution = 4 bits → $2^4 = 16$ levels
- Step size = $\frac{5V}{16} = 0.3125V$
- Given Vin = 1.2V

Each clock pulse increments the counter:

Clock	Counter	DAC Output (V)	Comparator Checks: Is DAC ≥ Vin?
1	0000	0.0000 V	No → Continue
2	0001	0.3125 V	No → Continue
3	0010	0.6250 V	No → Continue
4	0011	0.9375 V	No → Continue
5	0100	1.2500 V	Yes → Stop

Stop and Output

- DAC output just reached or exceeded Vin (1.25V ≥ 1.2V)
- The counter stops at `0100`
- Digital Output = 0100 (decimal 4)

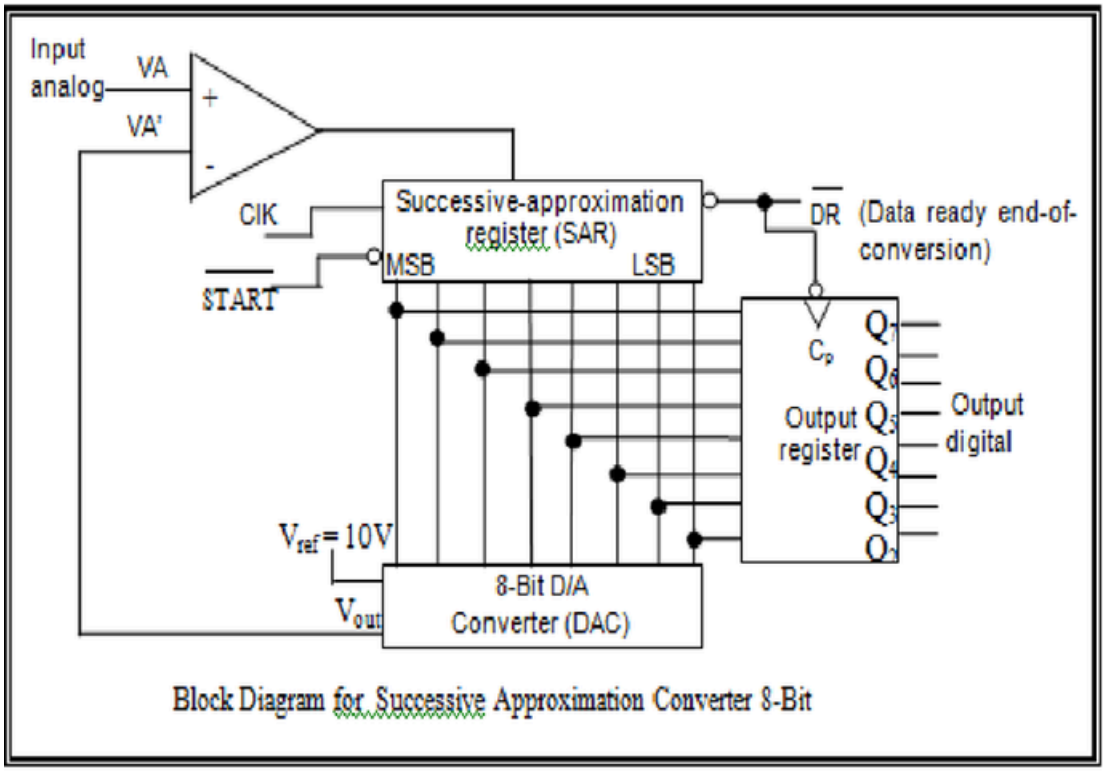
SUCCESSIVE APPROXIMATION CONVERTER (SAC)

1.SAC converts an analogue input signal to a digital output by successively approximating the value, bit by bit, from the most significant bit (MSB) to the least significant bit (LSB).

2.SAC has a shorter conversion time and a fixed (not dependent on the value of analogue input).

3.SAC main components;
i. Comparator.
ii. Successive Approximation Register (SAR).
iii. DAC (Digital-to-Analogue Converter).
iv. Output register.

GENERAL OPERATION SAC



Block Diagram for Successive Approximation Converter 8-Bit

1.Starting with the MSB, each bit in the successive approximation register (SAR) is activated and tested by the digital-to-analogue converter (DAC).

2.After each test, the DAC produces an output voltage that represents the bit.

3.The comparator compares this voltage with the input signal. If the input is larger, the bit is retained; otherwise it is reset (0).

EXAMPLE

SAC 4-bit with 1V step size was used to convert the input value, VA = 9.9 V. Show each step of the conversion.

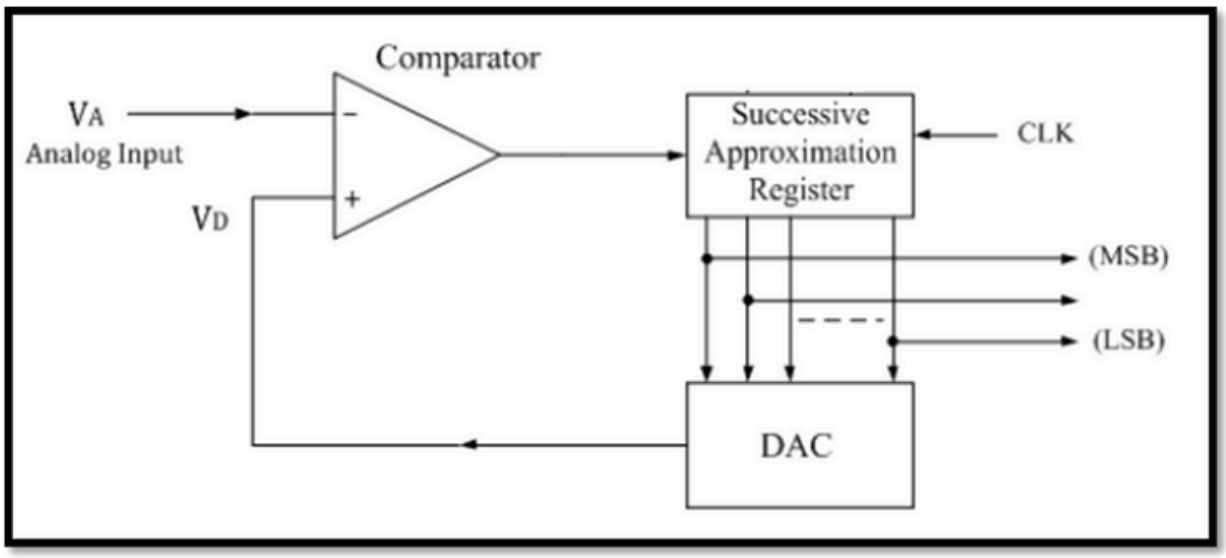
•Referring to the table, it is evident that each bit is tested sequentially until the DAC output voltage VA' > VA.

•However, the conversion does not depend on the input voltage; the conversion time is fixed for the Successive Approximation Converter (SAC).

Conversion Process For V_A = 9.9 V using SAC 4-Bit

Step	Registrar	VA' (V)	V_A (V)	Comparator
Initial conditions	0000	0	9.9	'1'
Set MSB to '1', VA' < V_A	1000	8	9.9	'1'
Set bit at bit 2 and remains the next bit, VA' > V_A	1100	12	9.9	'0'
Reset bit at bit 2 and set the next bit, VA' > VA	1010	10	9.9	'0'
Reset bit at bit 3 and set the LSB,VA' < VA	1001	9	9.9	'1'
Output of the show	1001			

SAC OPERATION



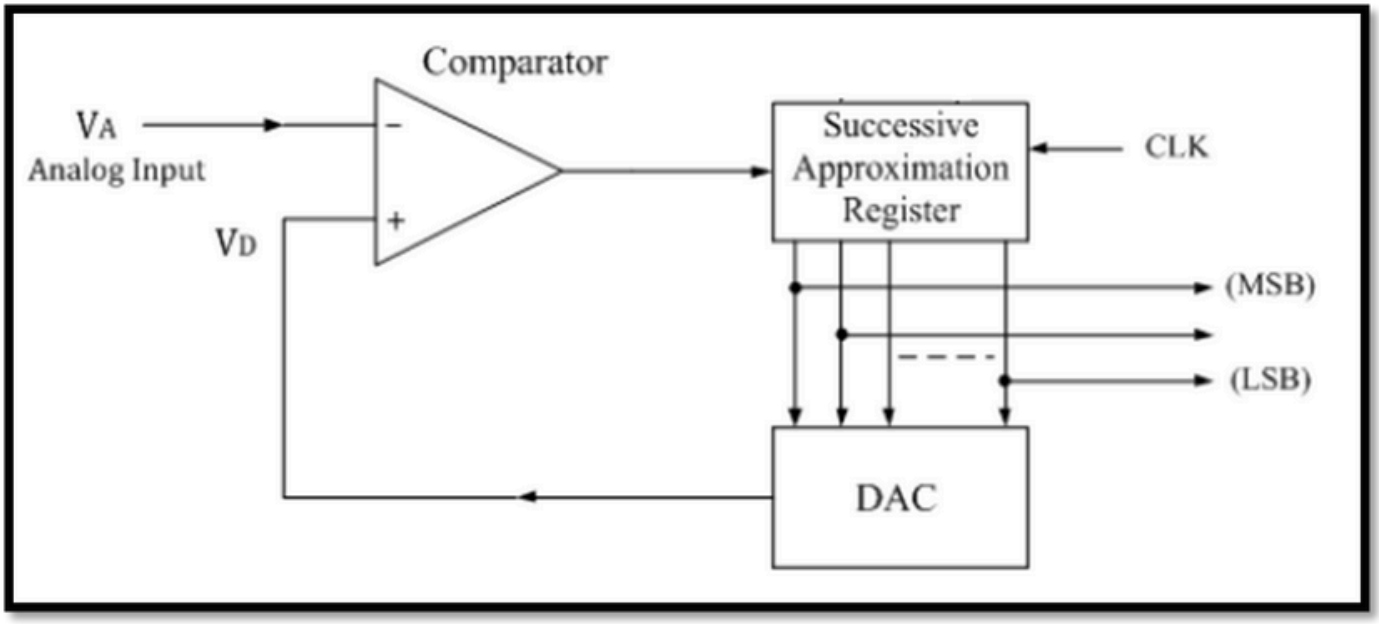
1.SAR ADC converts from MSB to LSB: When the conversion starts, the successive approximation register sets the most significant bit to 1 and all other bits to 0.

2.The input voltage will be compared to a reference voltage, and based on the output of the comparator, the successive approximation register (SAR) will adjust its output accordingly.

3.If *V*in in is greater than the DAC output, the most significant bit (MSB) remains set, and the next bit is set 1. If the input voltage is less than the DAC value, the most significant bit will be set to 0, and the next bit will be set to 1 for a new comparison.

4.Now, if the DAC voltage is less than the input voltage, the next bit before the most significant bit will set to one, and other bits will set to 0, this process will continue until the value closest to the input voltage reaches.

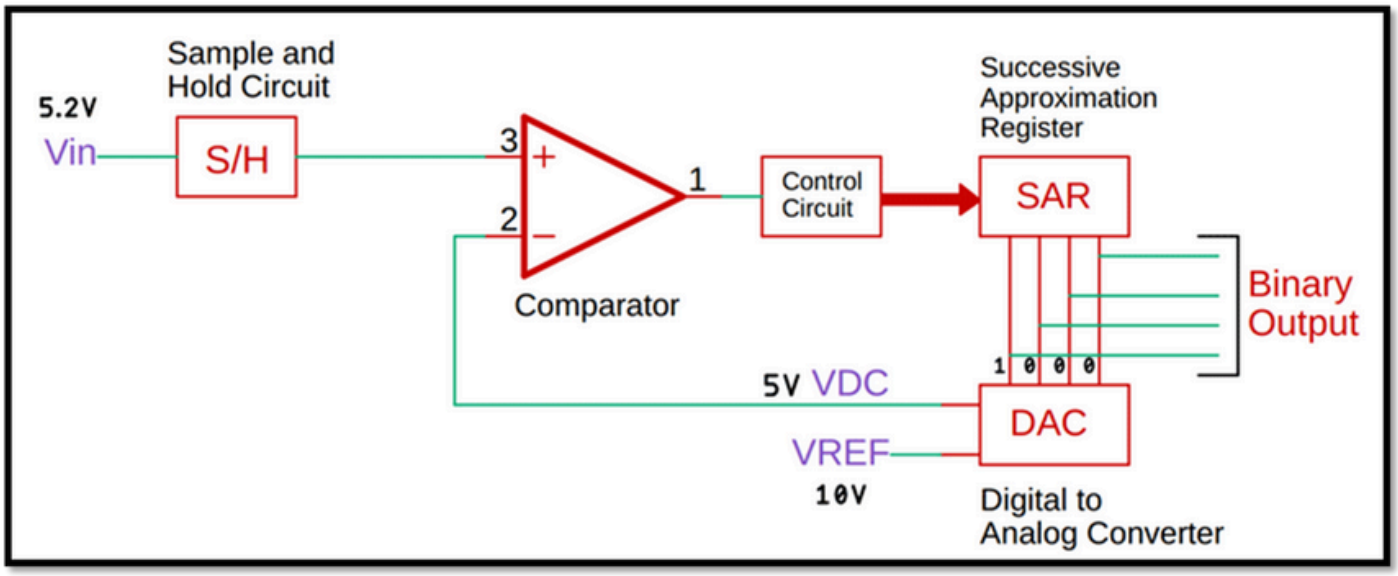
EXAMPLE



- **Resolution:** 4-bit → $2^4 = 16$ levels
- **Reference Voltage (Vref):** 5V
- **Step Size:** $\frac{5V}{16} = 0.3125V$
- **Input Voltage (Vin):** 2.7V

Step	SAR Register (Guess)	DAC Output (V)	Comparator: Vin > DAC?
1	`1000` (8)	$8 \times 0.3125 = 2.5V$	2.7V > 2.5V → Yes
2	`1100` (12)	$12 \times 0.3125 = 3.75V$	2.7V < 3.75V → No
3	`1010` (10)	$10 \times 0.3125 = 3.125V$	2.7V < 3.125V → No
4	`1001` (9)	$9 \times 0.3125 = 2.8125V$	2.7V < 2.8125V → No

EXAMPLE



Given:

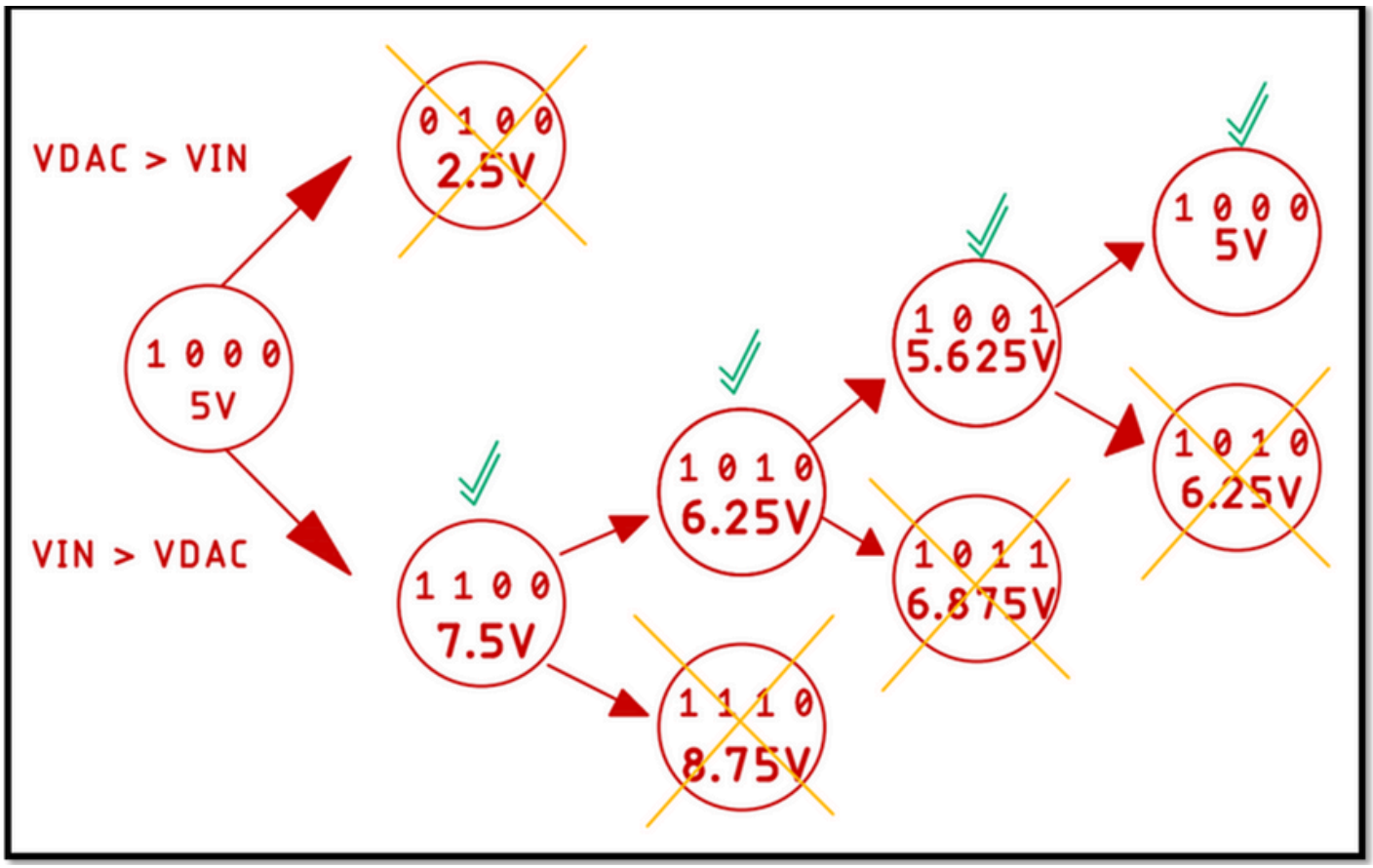
- **Vin** = 5.2 V
- **Vref** = 10 V
- **Resolution** = 4-bit
- **Total Digital Levels** = $2^4 = 16$
- **Step Size** = $\frac{10}{16} = 0.625\,V$

We will convert **Vin = 5.2 V** into its **4-bit digital output.**

Step-by-Step SAR Process:

We test each bit from **MSB to LSB**, using an internal DAC and comparator.

Step	Bit Tested	SAR Trial Code	Decimal Value	DAC Output (V)	Vin (5.2 V) > DAC?
1	MSB (bit 3)	`1000`	8	$8 \times 0.625 = 5.000\text{V}$	5.2 V > 5.0 V → Yes
2	Bit 2	`1100`	12	$12 \times 0.625 = 7.5\text{V}$	5.2 V < 7.5 V → No
3	Bit 1	`1010`	10	$10 \times 0.625 = 6.25\text{V}$	5.2 V < 6.25 V → No
4	Bit 0	`1001`	9	$9 \times 0.625 = 5.625\text{V}$	5.2 V < 5.625 V → No



ADC – TIME CONVERSION (TC MAX)

Conversion time is the time taken to convert the analogue input into a digital output.

$$T_{cmax} = (2^n - 1)\ clk/cyle$$

$$= \text{Total step} \times T_{input}$$

$$T_{input} = 1 / frequency$$

(f = clock frequency)

$T_{C\,(max)}$, the maximum conversion time occurs when $V_A \geq V_{FS}$.

$$Tc(ave) = T_{C\,(max)} / 2 \approx (2^n - 1)\ clk/cycle$$

To make the conversion, n-bit SAC requires n cycles bell-shaped, without determined by VA.
–This is because the control circuit will try every bit.

$$T_{cmax} = n\ X\ (1\ clock\ cycle)$$

EXAMPLE

Now let us compare the maximum conversion time Tc for the DRC and SAC 10-bit, given the clock frequency is 500 kHz.

$$f_{in} = \frac{1}{T_{in}} \Rightarrow T_{in} = \frac{1}{f_{in}} = \frac{1}{500k} = 2\mu s$$

For **DRC**, $Tc_{max} = (2^n - 1)$ X (1 clock cycle) = 1023 X 2μs = **2046 s**

For **SAC**, Tc_{max} = n X (1 clock cycle) = 10 X 2μs = **20 s**

From the comparison above we have found that SAC is 100 times faster than the DRC

THE DIFFERENCES BETWEEN SAC AND DRC

SAC	DRC
The fixed conversion (follow no. of bit)	Time conversion in accordance with Va
Tcmax = n bits x T 1 cycle, more speed (tc=time conversion)	Tcmax X 1 = number of cycle steps, the higher the longer the conversion of Va
Circuit using register	Circuit using counter

THE DIFFERENCES BETWEEN DAC AND ADC

DAC	ADC
Converts digital binary codes to continuous analogue signals.	Converts continuous analogue signals to digital signals.
The input is digital values and the output is an analogue signal.	The input is an analogue signal and the output is digital values.
The two main types of DAC circuits are Binary Weighted Resistor and R-2R Ladder.	The two main types of ADC circuits are Digital Ramp Converter and Successive Approximation Converter .

EXERCISE

1. List FOUR (4) main parts of Digital Ramp Converter.
2. With the aid of diagram, explain the differences between R-2R circuit and Binary Weighted Resistor.
3. State the function of an Analogue to digital Converter (ADC) and list TWO (2) types of ADC.
4. Explain the differences between R-2R Ladder circuit and a Binary Weighted Resistor.
5. Identify TWO (2) circuit of an Analogue to Digital Converter (ADC) and Digital to Analogue Converter (DAC).
6. Compare THREE (3) differences between Analogue to Digital Converter (ADC) and Digital to Analogue Converter (DAC).
7. List FOUR (4) main parts of the Digital Ramp Converter.

EXERCISE

1. Calculate the successive approximation converter (SAC) digital value with 4 bits input register number. Given Vin = 2.3V and the step size is 1.5. (FE S1 2022/2023)

ANSWER:

- **Vin** = 2.3 V
- **Step size** = 1.5
- **Input register bits** = 4 bits → So, output range: 0 to 15 (since $2^4 = 16$)

SAR Register	Vo (DAC Output)	Compare with Vin	Comparator
0000	0	0 < 2.3	1 (set)
1000	8 x 1.5 = 12	12 > 2.3	0 (reset)
0100	4 x 1.5 = 6	6 > 2.3	0 (reset)
0010	2 x 1.5 = 3	3 > 2.3	0 (reset)
0001	1 x 1.5 = 1.5	1.5 < 2.3	1 (hold)

2. Digital to Analogue converter 5 bits with step size of 10mV. Calculate for full scale voltage and a percent resolution. Draw a 3 bits system of R-2R Ladder circuit to perform Digital to Analogue conversion. (FE S1 2023/2024)

ANSWER:

Number of bits = 5

Step size = 10mV

Total step = $2^n - 1$ = 31 steps

Full scale output voltage = total step x step size

= 31 x 10mV = 0.31V

$$\text{Percent Resolution} = \left(\frac{\text{Step Size}}{\text{Full Scale Voltage}}\right) \times 100$$

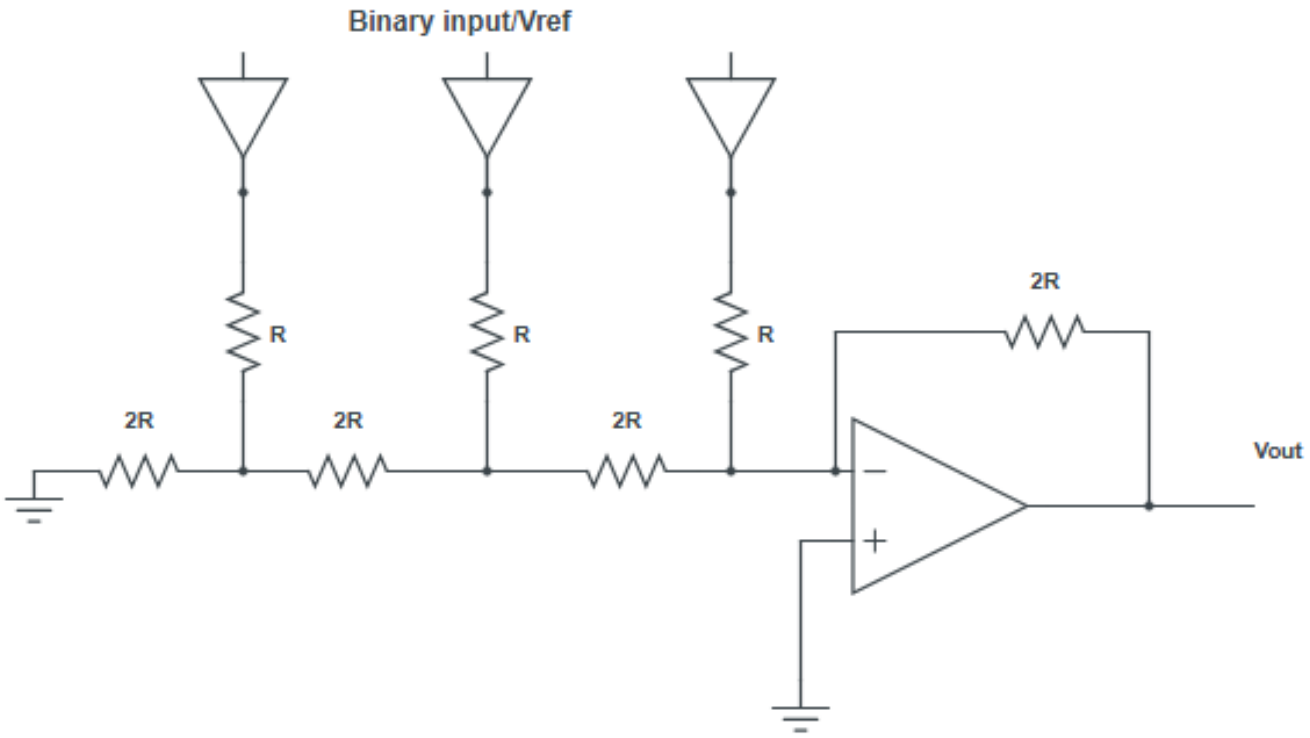
$$= \left(\frac{0.01}{0.31}\right) \times 100 \approx \boxed{3.23\%}$$

or

$$\text{Percent Resolution} = \left(\frac{1}{2^N - 1}\right) \times 100$$

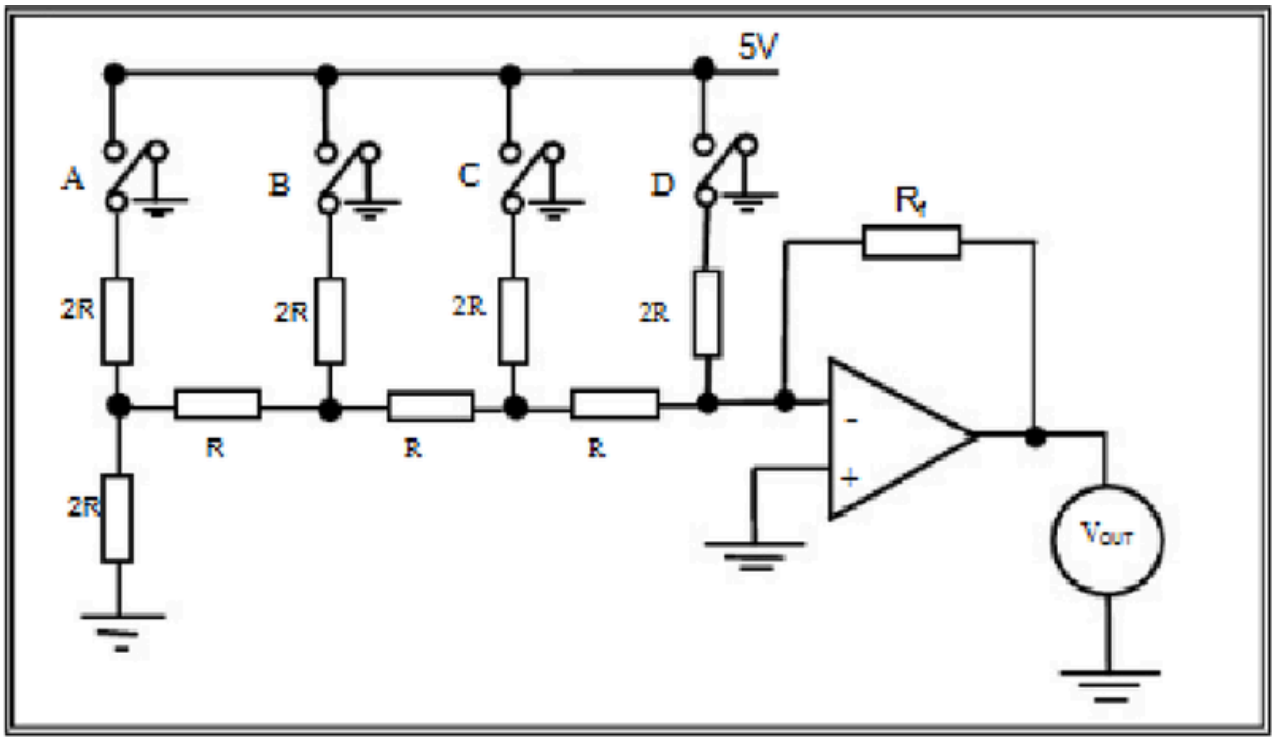
$$\text{Percent Resolution} = \left(\frac{1}{31}\right) \times 100 \approx \boxed{3.23\%}$$

EXERCISE



3. By drawing a 4 bits R-2R Ladder circuit diagram with given values of RF = R = 1KΩ and Vref = 5V , calculate the output voltage for input 1001, 1011 and 1000 (binary bits). (FE S2 2023/2024)

ANSWER:



$$\text{Vout} = -\frac{Vref}{2^n} + \frac{RF}{R}\ x\ Bin$$

Input = 1001 (binary) = 9 (decimal)

$$\text{Vout} = -\frac{Vref}{2^n} x \frac{RF}{R}\ x\ Bin$$

$$\text{Vout} = -\frac{5V}{2^4} x \frac{1K}{1K}\ x\ 9$$

$$\text{Vout} = -2.8125V$$

Input = 1011 (binary) = 11 (decimal)

$$\text{Vout} = -\frac{Vref}{2^n} x \frac{RF}{R}\ x\ Bin$$

$$\text{Vout} = -\frac{5V}{2^4} x \frac{1K}{1K}\ x\ 11$$

$$\text{Vout} = -3.4375V$$

Input = 1000 (binary) = 8 (decimal)

$$\text{Vout} = -\frac{Vref}{2^n} x \frac{RF}{R}\ x\ Bin$$

$$\text{Vout} = -\frac{5V}{2^4} x \frac{1K}{1K}\ x\ 8$$

$$\text{Vout} = -2.5V$$

EXERCISE

- **R** = 1 kΩ
- **Rf** (feedback resistor) = 1 kΩ
- **Vref** = 5 V

🔷 **Input:** `1001`

$$V_{out} = 5 \times \left(\frac{1}{2} + \frac{0}{4} + \frac{0}{8} + \frac{1}{16}\right) = 5 \times (0.5 + 0 + 0 + 0.0625) = 5 \times 0.5625 = \boxed{2.8125\ \text{V}}$$

🔷 **Input:** `1011`

$$V_{out} = 5 \times \left(\frac{1}{2} + \frac{0}{4} + \frac{1}{8} + \frac{1}{16}\right) = 5 \times (0.5 + 0 + 0.125 + 0.0625) = 5 \times 0.6875 = \boxed{3.4375\ \text{V}}$$

🔷 **Input:** `1000`

$$V_{out} = 5 \times \left(\frac{1}{2} + \frac{0}{4} + \frac{0}{8} + \frac{0}{16}\right) = 5 \times 0.5 = \boxed{2.5\ \text{V}}$$

EXERCISE

4. Given a 4 bits Successive Approximation Converter with step size of 0.5V is used to convert an input voltage, VA =5.6V. Explain the steps for each conversion process. (FE S1 2024/2025)

ANSWER:

- **4-bit SAR ADC** → can represent $2^4 = 16$ levels.
- **Step size = 0.5V**
- Therefore, the full range of the ADC is:

$$\text{Range} = 0V \text{ to } (16 - 1) \times 0.5V = 7.5V$$

- **Input voltage VA = 5.6V**

SAR Register	Vo (DAC Output)	Compare with Vin	Comparator
0000	0	0 < 5.6	1 (set)
1000	8 x 0.5 = 4	4 < 5.6	1 (set)
1100	12 x 0.5 = 6	6 > 5.6	0 (reset)
1010	10 x 0.5 = 5	5 < 5.6	1 (set)
1011	11 x 0.5 = 5.5	5.5 < 5.6	1 (hold)

5. A R-2R circuits is design with a reference voltage of -15V and the feedback resistor RF is equal to the fixed resistor R. Calculate the number of input bits for this converter if the equivalent analogue value is 7.5V for a digital value of 8 (decimal). (FE S1 2024/2025)

ANSWER:

Given:

Vref = -15V

Vout = 7.5V

Bin = 8 (decimal)

$$\text{Vout} = -\frac{Vref}{2^n} x \frac{RF}{R} \; x \; Bin$$

$$7.5\text{V} = -\frac{-5V}{2^n} x \frac{Rf}{R} \; x \; 8$$

$$7.5\text{V} = \frac{120}{2^n}$$

$$2^n = 16$$

$$n = 4$$

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