

**SECTION A: 60 MARKS**  
**BAHAGIAN A: 60 MARKAH**

**INSTRUCTION:**

This section consists of **FOUR (4)** structured questions. Answers **ALL** questions.

**ARAHAN:**

*Bahagian ini mengandungi EMPAT (4) soalan berstruktur. Jawab SEMUA soalan.*

**QUESTION 1**

**SOALAN 1**

C LO1  
C1

- (a) Define the Integrated Circuit.  
*Definisikan Litar Bersepadu.*

[2 marks]  
 [2 markah]

CLO1  
C2

- (b) Integrated Circuit can be classified into four categories. Describe **THREE (3)** classification of integrated circuit based on circuit function.  
*Litar Bersepadu boleh diklasifikasikan kepada empat kategori. Huraikan TIGA (3) klasifikasi litar bersepadu berdasarkan fungsi litar.*

[6 marks]  
 [6 markah]

CLO1  
C2

- (c) Floating Zone or Czochralski methods can be used to grow the single crystal. Explain briefly the process of Czochralski method.  
*Kaedah Zon Terapung atau Czochralski boleh digunakan untuk menghasilkan hablur tunggal. Terangkan secara ringkas tentang kaedah Czochralski.*

[7 marks]  
 [7 markah]

**QUESTION 2**

**SOALAN 2**

CLO1  
C1

- (a) Draw the symbol of PMOS and NMOS transistors.  
*Lukiskan simbol untuk transistor PMOS dan transistor NMOS.*

[2 marks]  
 [2 markah]

- CLO1  
C3
- (b) Sketch the cross section of PMOS and NMOS transistors with the labels.  
*Lakarkan keratan rentas bagi transistor PMOS dan transistor NMOS dengan label.*
- [6 marks]  
[6 markah]

- CLO1  
C3
- (c) Propagation delay is one of the characteristic parameters of CMOS inverter. Interpret the propagation delay characteristics with the aid of a suitable diagram.  
*Lengah perambatan adalah salah satu ciri parameter bagi penyongsang CMOS. Tafsirkan ciri-ciri lengah perambatan dengan bantuan gambarajah yang sesuai.*
- [7 marks]  
[7 markah]

**QUESTION 3**

**SOALAN 3**

- CLO2  
C3
- (a) Based on the Figure A3(a), draw the static CMOS circuit.  
*Berdasarkan Rajah A3(a), lukiskan litar CMOS statik.*

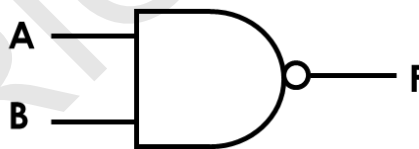


Figure A3(a) / Rajah A3(a)

[5 marks]  
[5 markah]

- CLO2  
C3
- (b) Illustrate a Pseudo NMOS schematic logic diagram for 2- input NAND gate.  
*Ilustrasi gambarajah logik skematik Pseudo NMOS bagi get TAK DAN 2-masukan.*

[5 marks]  
[5 markah]

- CLO2  
C3
- (c) Interpret **TWO (2)** major phases in dynamic logic circuit.  
*Tafsirkan DUA (2) fasa utama dalam litar logik dinamik.*

[5 marks]  
[5 markah]

## QUESTION 4

## SOALAN 4

- CLO1  
C1 (a) State the characteristics of Application Specific Integrated Circuits (ASICs).  
*Nyatakan ciri – ciri bagi Litar Bersepadu Khusus (ASICs).*
- [2 marks]  
[2 markah]
- CLO1  
C3 (b) Interpret the differences between Programmable Logic Devices (PROM), Programmable Array Logic (PAL) and Programmable Logic Array (PLA).  
*Tafsirkan perbezaan di antara Programmable Logic Devices (PROM), Programmable Array Logic (PAL) dan Programmable Logic Array (PLA).*
- [6 marks]  
[6 markah]
- CLO1  
C3 (c) Based on Programmable Logic Array architecture in Figure A4(c), interpret the output equation for  $f_1$ ,  $f_2$  and  $f_3$ .  
*Berdasarkan rekabentuk seni bina Programmable Logic Array dalam Rajah A4(c), tafsirkan persamaan keluaran bagi  $f_1$ ,  $f_2$  dan  $f_3$ .*

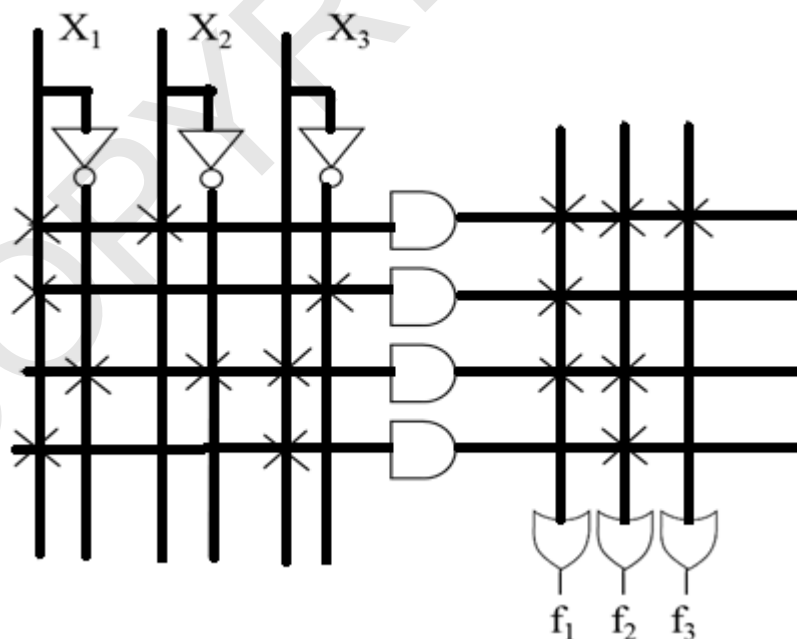


Figure A4(c) / Rajah A4(c)

[7 marks]  
[7 markah]

**SECTION B: 40 MARKS****BAHAGIAN B: 40 MARKAH****INSTRUCTION:**

This section consists of **TWO (2)** essay questions. Answer **ALL** questions.

**ARAHAN:**

Bahagian ini mengandungi **DUA (2)** soalan esei. Jawab **SEMUA** soalan.

**QUESTION 1****SOALAN 1**

CLO2  
C3

Draw a static CMOS logic circuit and stick diagram for the following logic function :

*Lukiskan litar logik CMOS statik dan rajah lidi untuk fungsi logik berikut :*

$$\overline{(A + B) \cdot (C \cdot D)}$$

[20 marks]  
[20 markah]

**QUESTION 2****SOALAN 2**

CLO2  
C5

By using Pull-Up Network (PUN) and Pull-Down Network (PDN), construct a static CMOS circuit based on the Boolean equation  $Z1 = \overline{\overline{A} \overline{B} + AB}$  and  $Z2 = \overline{AB + AC}$ .

*Dengan menggunakan Rangkaian Tarik Atas (PUN) dan Rangkaian Tarik Bawah (PDN), bina satu litar CMOS statik bagi persamaan Boolean  $Z1 = \overline{\overline{\overline{A} \overline{B} + AB}}$  dan  $Z2 = \overline{AB + AC}$ .*

[20 marks]  
[20 markah]

**SOALAN TAMAT**