SULIT

KEMENTERIAN PENDIDIKAN TINGGI
JABATAN PENDIDIKAN POLITEKNIK DAN KOLEJ KOMUNITI

BAHAGIAN PEPERIKSAAN DAN PENILAIAN
JABATAN PENDIDIKAN POLITEKNIK DAN KOLEJ KOMUNITI
KEMENTERIAN PENDIDIKAN TINGGI

JABATAN KEJURUTERAAN ELEKTRIK

PEPERIKSAAN AKHIR

SESI II : 2024/2025

DEC30043: MICROPROCESSOR FUNDAMENTALS

TARIKH : 18 MEI 2025
MASA : 8.30 PAGI – 10.30 PAGI (2 JAM)

Kertas soalan ini mengandungi **LAPAN (8)** halaman bercetak.
Bahagian A: Subjektif (4 soalan)
Bahagian B: Esei (1 soalan)
Dokumen sokongan yang disertakan : STM32 GPIO Reference Manual

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JANGAN BUKA KERTAS SOALAN INI SEHINGGA DIARAHKAN

(CLO yang tertera hanya sebagai rujukan)

SECTION A: 80 MARKS
BAHAGIAN A: 80 MARKAH

INSTRUCTIONS:

This section consists of **FOUR (4)** subjective questions. Answer **ALL** questions.

ARAHAN:

*Bahagian ini mengandungi **EMPAT (4)** soalan subjektif. Jawab **SEMUA** soalan.*

QUESTION 1

SOALAN 1

CLO1 (a) Describe **TWO (2)** bus function in ARM processor.
*Huraikan **DUA (2)** fungsi bas dalam pemproses ARM.*

[4 marks]
[4 markah]

CLO1 (b) Explain the data movement for every instructions in Table A1(b) after it has been executed.
Terangkan pergerakan data yang berlaku pada setiap arahan dalam Jadual A1(b) selepas ia dilaksanakan.

Table A1(b)/Jadual A1(b)

Instruction	Data Movement Explanation
MOVS R2, #54	
MOVS R1, R3	
LDR R4, #0x5577BBCC	

[6 marks]
[6 markah]

CLO1

(c) Based on the assembly language given, solve instruction in Table A1(c) to demonstrate how it will work. The initial value of Register R3=0x0000DFEB and R4=0x00000002.

Berdasarkan bahasa himpunan yang diberikan, selesaikan instruction dalam Table A1(c) untuk menunjukkan cara ia berfungsi. Nilai awal daftar R3=0x0000DFEB dan R4=0x00000002

Table A1(c)/ *Jadual A1(c)*

Bil	Instruction
i.	ANDS R3, R3, R4
ii.	RORS R3, R3, R4

[10 marks]

[10 markah]

QUESTION 2

SOALAN 2

CLO1 *(a)* The Cortex-M processors have several advantages. State **TWO (2)** advantages of Cortex-M.

*Pemproses Cortex-M mempunyai beberapa kelebihan. Nyatakan **DUA (2)** kelebihan Cortex-M.*

[4 marks]

[4 markah]

CLO1 (b) Convert a comment statements in Table A2(b) to instructions in ARM assembly language.

Tukarkan pernyataan dalam ulasan dalam Jadual A2(b) kepada arahan dalam bahasa himpunan ARM.

Table A2(b)/ *Jadual A2(b)*

Comment/*Ulasan*	Instruction/*Arahan*
Insert immediate decimal data 235 into register R4, flags are not updated	
Insert immediate Hexadecimal data 23AD into register R5, flags get updated	
Insert data from register R3 into R1, flags are not updated	

[6 marks]

[6 markah]

(c) Write a program that executes the process described by the flowchart in Figure A2(c)
Tulis arahan yang melaksanakan proses yang diterangkan oleh carta alir dalam Rajah A2(c).

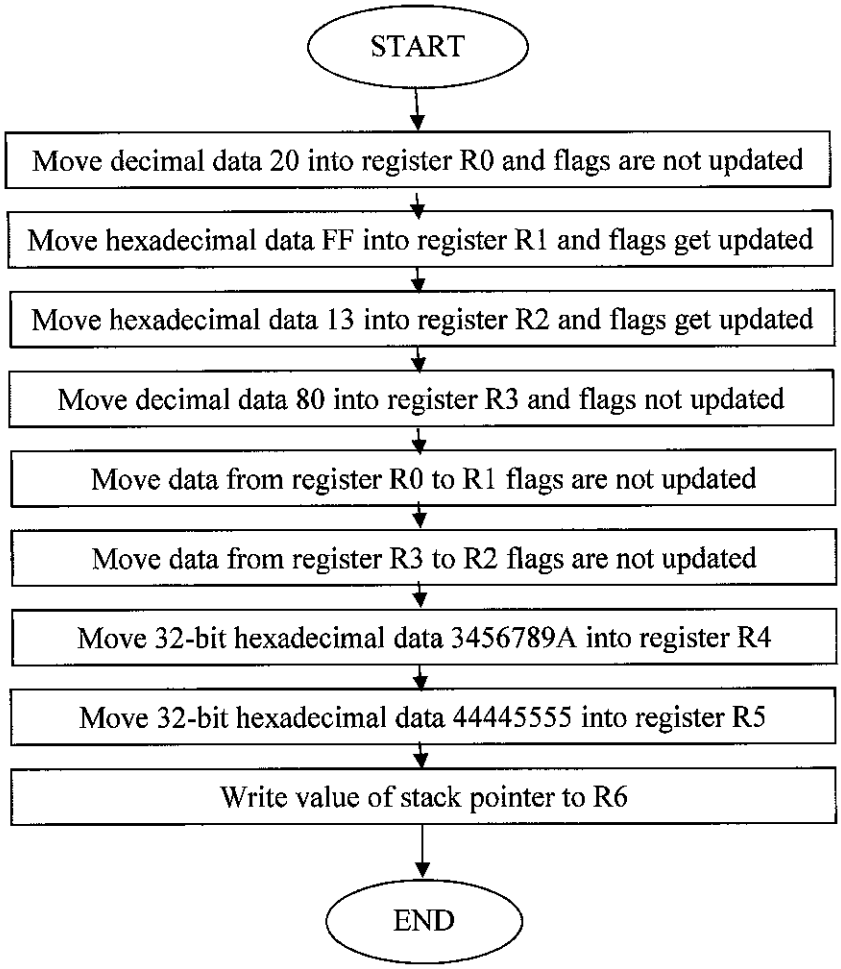

Figure A2(c)/ *Rajah A2(c)*

[10 marks]
[10 markah]

CLO1

QUESTION 3

SOALAN 3

(a) List any **FOUR (4)** branch instructions assembly code with its description

*Senaraikan mana-mana **EMPAT (4)** kod pemasangan arahan cabangan berserta dengan penerangan ringkasnya.*

[4 marks]

[4 markah]

CLO1

(b) Interpret the assembly instructions in Table A3(b) in the form of arithmetic operation (arithmetic equation).

Tafsirkan arahan pemasangan dalam Jadual A3(b) dalam bentuk operasi aritmetik.

Table A3(b)/ *Jadual A3(b)*

Assembly Instructions	Arithmetic Operation
ADD R0, R0, R1	
ADDS R0, R0, #0x12	
SUB R2, R2, R0	
SUBS R1, R1, #4	
MULS R4, R5, R4	
MULS R3,R1,R2	

[6 marks]
[6 markah]

CLO1

(c) With the aids of a suitable flow chart, write an ARM Assembly language program to calculate the area of rectangle in Figure A3(c).

Dengan bantuan carta alir yang sesuai, tulis pengaturcaraan bahasa himpunan ARM untuk mengira luas segi empat tepat dalam Rajah A3(c).

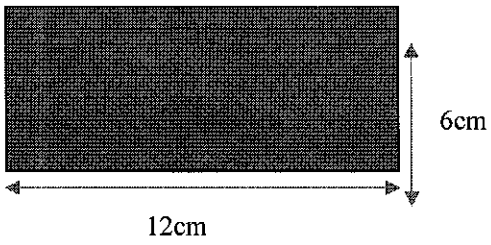

Figure A3(c)/ *Rajah A3(c).*

[10 marks]
[10 markah]

CLO1

QUESTION 4

SOALAN 4

(a) Explain the basic branch instruction for Unconditional Branch and Conditional Branch with an example.

Terangkan arahan asas cabang untuk CabangTidak Bersyarat dan Cabang Bersyarat dengan contoh.

[6 marks]

[*6 markah*]

CLO1

(b) Data processing instructions change the flags in the APSR. Explain the flag bit in APSR that influences the conditional branches.

Arahan pemprosesan data menukar bendera dalam APSR. Terangkan bit bendera dalam APSR yang boleh digunakan untuk cawangan bersyarat.

[6 marks]

[*6 markah*]

CLO1

(c) By referring to STM32 Reference Manual (in Appendix), write an instruction using C language to configure GPIO in Table A4(c).

Dengan merujuk kepada STM32 GPIO Manual Rujukan (Appendix), Tulis araham program menggunakan Bahasa C untuk menetapkan GPIO dalam Jadual A4(c).

Table A4(c).

GPIO Configuration	**Instruction**
Enable Clock for GPIOA	
Enable Clock for GPIOC	
Set GPIO PA5 as INPUT	
Set GPIO PC8 as OUTPUT	

[8 marks]

[*8 markah*]

SECTION B : 20 MARKS
BAHAGIAN B : 20 MARKAH

INSTRUCTION:

This section consists of **ONE (1)** essay question. Answer the questions.

ARAHAN:

Bahagian ini mengandungi **SATU (1)** soalan esei. Jawab soalan tersebut.

QUESTION 1

SOALAN 1

CLO1

By Referring to *Figure B1* and the **STM32 GPIO Reference Manual**, write a C program that controls a Green LED based on the state of a push button switch. The LED should **turn ON** when the switch is pressed and **turn OFF** when the switch is released. Ensure the following pin configurations:

- **PA5** is configured as a **digital output** pin (connected to the Green LED).
- **PC13** is configured as a **digital input** pin (connected to the switch).

Dengan merujuk kepada Rajah B1 dan Manual Rujukan STM GPIO, tulis satu program C yang mengawal LED Hijau berdasarkan keadaan suis. LED Hijau akan menyala apabila suis ditekan dan padam apabila suis dilepaskan. Pastikan konfigurasi pin berikut:

- *PA5 ditetapkan sebagai pin keluaran digital (disambungkan ke LED Hijau).*
- *PC13 ditetapkan sebagai pin masukan digital (disambungkan ke suis).*

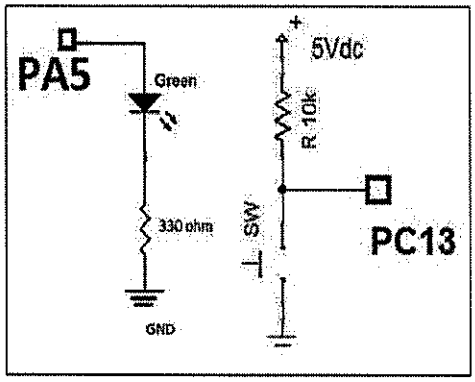

Figure B1

[20 marks]
[*20 markah*]

SOALAN TAMAT

life.augmented

RM0377
Reference manual

Ultra-low-power STM32L0x1 advanced Arm®-based 32-bit MCUs

Introduction

This reference manual targets application developers. It provides complete information on how to use the STM32L0x1 microcontroller memory and peripherals.

The STM32L0x1 is a line of microcontrollers with different memory sizes, packages and peripherals.

For ordering information, mechanical and electrical device characteristics please refer to the corresponding datasheets.

For information on the Arm® Cortex®-M0+ core, refer to the *Cortex®-M0+ Technical Reference Manual*.

The STM32L0x1 microcontrollers include state-of-the-art patented technology.

Related documents

- Cortex®-M0+ Technical Reference Manual, available from www.arm.com.
- STM32L0 Series Cortex®-M0+ programming manual (PM0223).
- STM32L0x1 datasheets.
- STM32L0x1 erratasheet.

Bits 3:2 Reserved, must be kept at reset value.

Bit 1 **TIM3RST:** Timer3 reset
Set and cleared by software.
0: No effect
1: Resets timer3

Bit 0 **TIM2RST:** Timer2 reset
Set and cleared by software.
0: No effect
1: Resets timer2

7.3.11 GPIO clock enable register (RCC_IOPENR)

Address: 0x2C

Reset value: 0x0000 0000

Access: no wait state, word, half-word and byte access

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	IOPH EN	Res.	Res.	IOPE EN	IOPD EN	IOPC EN	IOPB EN	IOPA EN
								rw			rw	rw	rw	rw	rw

Bits 31:8 Reserved, must be kept at reset value.

Bit 7 **IOPHEN:** I/O port H clock enable bit
This bit is set and cleared by software.
0: port H clock disabled
1: port H clock enabled

Bits 6:45 Reserved, must be kept at reset value.

Bit 4 **IOPEEN:** I/O port E clock enable bit
This bit is set and cleared by software.
0: port E clock disabled
1: port E clock enabled

Bit 3 **IOPDEN:** I/O port D clock enable bit
This bit is set and cleared by software.
0: port D clock disabled
1: port D clock enabled

8 General-purpose I/Os (GPIO)

8.1 Introduction

Each general-purpose I/O port has four 32-bit configuration registers (GPIOx_MODER, GPIOx_OTYPER, GPIOx_OSPEEDR and GPIOx_PUPDR), two 32-bit data registers (GPIOx_IDR and GPIOx_ODR) and a 32-bit set/reset register (GPIOx_BSRR). In addition all GPIOs have a 32-bit locking register (GPIOx_LCKR) and two 32-bit alternate function selection registers (GPIOx_AFRH and GPIOx_AFRL).

8.2 GPIO main features

- Output states: push-pull or open drain + pull-up/down
- Output data from output data register (GPIOx_ODR) or peripheral (alternate function output)
- Speed selection for each I/O
- Input states: floating, pull-up/down, analog
- Input data to input data register (GPIOx_IDR) or peripheral (alternate function input)
- Bit set and reset register (GPIOx_ BSRR) for bitwise write access to GPIOx_ODR
- Locking mechanism (GPIOx_LCKR) provided to freeze the I/O port configurations
- Analog function
- Alternate function selection registers
- Fast toggle capable of changing every two clock cycles
- Highly flexible pin multiplexing allows the use of I/O pins as GPIOs or as one of several peripheral functions

8.3 GPIO functional description

Subject to the specific hardware characteristics of each I/O port listed in the datasheet, each port bit of the general-purpose I/O (GPIO) ports can be individually configured by software in several modes:

- Input floating
- Input pull-up
- Input-pull-down
- Analog
- Output open-drain with pull-up or pull-down capability
- Output push-pull with pull-up or pull-down capability
- Alternate function push-pull with pull-up or pull-down capability
- Alternate function open-drain with pull-up or pull-down capability

Each I/O port bit is freely programmable, however the I/O port registers have to be accessed as 32-bit words, half-words or bytes. The purpose of the GPIOx_BSRR register is to allow atomic read/modify accesses to any of the GPIOx_ODR registers. In this way, there is no risk of an IRQ occurring between the read and the modify access.

8.3.15 BOOT0/GPIO pin sharing

On category 1 devices, the BOOT0 pin is shared with a GPIO pin. The BOOT0 pin input level can be read as an input value on the shared GPIO pin. This pin features specific input voltage characteristics (refer to the corresponding datasheet for more details).

8.4 GPIO registers

For a summary of register bits, register address offsets and reset values, refer to *Table 46*.

The peripheral registers can be written in word, half word or byte mode.

8.4.1 GPIO port mode register (GPIOx_MODER) (x =A to E and H)

Address offset:0x00

Reset value: 0xEBFF FCFF for port A

Reset value: 0xFFFF FFFF for the other ports

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MODE15[1:0]		MODE14[1:0]		MODE13[1:0]		MODE12[1:0]		MODE11[1:0]		MODE10[1:0]		MODE9[1:0]		MODE8[1:0]	
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MODE7[1:0]		MODE6[1:0]		MODE5[1:0]		MODE4[1:0]		MODE3[1:0]		MODE2[1:0]		MODE1[1:0]		MODE0[1:0]	
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 31:0 **MODE[15:0][1:0]:** Port x configuration I/O pin y (y = 15 to 0)
These bits are written by software to configure the I/O mode.
00: Input mode
01: General purpose output mode
10: Alternate function mode
11: Analog mode (reset state) .

8.4.2 GPIO port output type register (GPIOx_OTYPER) (x = A to E and H)

Address offset: 0x04

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OT15	OT14	OT13	OT12	OT11	OT10	OT9	OT8	OT7	OT6	OT5	OT4	OT3	OT2	OT1	OT0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 31:16 Reserved, must be kept at reset value.

Bits 15:0 **OT[15:0]:** Port x configuration I/O pin y (y = 15 to 0)
These bits are written by software to configure the I/O output type.
0: Output push-pull (reset state)
1: Output open-drain

8.4.3 GPIO port output speed register (GPIOx_OSPEEDR) (x = A to E and H)

Address offset: 0x08

Reset value: 0x0C00 0000 (for port A)

Reset value: 0x0000 0000 (for the other ports)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OSPEED15 [1:0]		OSPEED14 [1:0]		OSPEED13 [1:0]		OSPEED12 [1:0]		OSPEED11 [1:0]		OSPEED10 [1:0]		OSPEED9 [1:0]		OSPEED8 [1:0]	
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OSPEED7 [1:0]		OSPEED6 [1:0]		OSPEED5 [1:0]		OSPEED4 [1:0]		OSPEED3 [1:0]		OSPEED2 [1:0]		OSPEED1 [1:0]		OSPEED0 [1:0]	
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 31:0 **OSPEED[15:0][1:0]**: Port x configuration I/O pin y (y = 15 to 0)
These bits are written by software to configure the I/O output speed.
00: Low speed
01: Medium speed
10: High speed
11: Very high speed

Note: Refer to the device datasheet for the frequency specifications and the power supply and load conditions for each speed..

8.4.4 GPIO port pull-up/pull-down register (GPIOx_PUPDR) (x = A to E and H)

Address offset: 0x0C

Reset value: 0x2400 0000 (for port A)

Reset value: 0x0000 0000 (for the other ports)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PUPD15[1:0]		PUPD14[1:0]		PUPD13[1:0]		PUPD12[1:0]		PUPD11[1:0]		PUPD10[1:0]		PUPD9[1:0]		PUPD8[1:0]	
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PUPD7[1:0]		PUPD6[1:0]		PUPD5[1:0]		PUPD4[1:0]		PUPD3[1:0]		PUPD2[1:0]		PUPD1[1:0]		PUPD0[1:0]	
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 31:0 **PUPD[15:0][1:0]:** Port x configuration I/O pin y (y = 15 to 0)
These bits are written by software to configure the I/O pull-up or pull-down
00: No pull-up, pull-down
01: Pull-up
10: Pull-down
11: Reserved

8.4.5 GPIO port input data register (GPIOx_IDR) (x = A to E and H)

Address offset: 0x10

Reset value: 0x0000 XXXX

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bits 31:16 Reserved, must be kept at reset value.

Bits 15:0 **ID[15:0]:** Port x input data I/O pin y (y = 15 to 0)
These bits are read-only. They contain the input value of the corresponding I/O port.

8.4.6 GPIO port output data register (GPIOx_ODR) (x = A to E and H)

Address offset: 0x14

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OD15	OD14	OD13	OD12	OD11	OD10	OD9	OD8	OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 31:16 Reserved, must be kept at reset value.

Bits 15:0 **OD[15:0]:** Port output data I/O pin y (y = 15 to 0)
These bits can be read and written by software.
Note: For atomic bit set/reset, the OD bits can be individually set and/or reset by writing to the GPIOx_BSRR register (x = A..E and H).