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CMOS IC DESIGN & FABRICATION

WAN 'AMIRAH BASYARAH ZAINOL ABIDIN
MUHAMAD REDUAN ABU BAKAR
NORJULIANA OTHMAN

DEPARTMENT OF ELECTRICAL ENGINEERING

Editor
Wan 'Amira Basyarah Binti Zainol Abidin
Muhamad Reduan Bin Abu Bakar
Norjuliana Binti Othman

Writer
Wan 'Amira Basyarah Binti Zainol Abidin
Muhamad Reduan Bin Abu Bakar
Norjuliana Binti Othman

Designer
Wan 'Amira Basyarah Binti Zainol Abidin
Muhamad Reduan Bin Abu Bakar
Norjuliana Binti Othman

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Perlis

ABSTRACT

The electronics industry has achieved a phenomenal growth over the last few decades, due to the rapid advances in integration technologies and large-scale systems design. The use of integrated circuits in high-performance computing, telecommunications, and consumer electronics has been growing very fast. Typically, the required computational and information processing power of these applications is the driving force for the fast development of this field. Many component such as transistors, resistors, capacitors, inductors go through invention process by integrated circuit development technologies.

This book provides a comprehensive reference for invention of integrated circuits design. The author focuses equally on history of semiconductor devices. The author also tells about integrated circuit fabrication process which is starting with crystal structures. The aim of this book is to provide a knowledge of designing, fabricating, understanding, and testing a microchip. The content is structured to be very accessible and self-contained, allowing readers with diverse backgrounds to read and get a deep knowledge about CMOS development process.

ACKNOWLEDGEMENT

First of all, Alhamdulillah, thanks Almighty for His guidance and blessing. We had succeeded in completing the CMOS E-Book. We want to express our utmost gratitude to our Head Department of Electrical Engineering, Mr Shaffie Bin Husin, who supported us in grabbing this opportunity. Without his support, we would not be able to produce this E-Book. Not to forget the E-Learning team because it provides us with this opportunity and guides us in making this E-Book.

Besides, we also extend our gratitude to all friends and our lovely families for their kindness and sincere assistance in adding us to finish up this E-Book. Indeed, we have appreciated them. Again, thanks for everything.

Our hopes are may this E-Book helps students out there, especially engineering students in polytechnic, ease to understand and implements in their CMOS course. Nevertheless, we also need any comments from reads to help us improve our next debut. We hope this E-Book could ease everyone to understand and implement the knowledge and could fulfill everybody needs.

Thank you.

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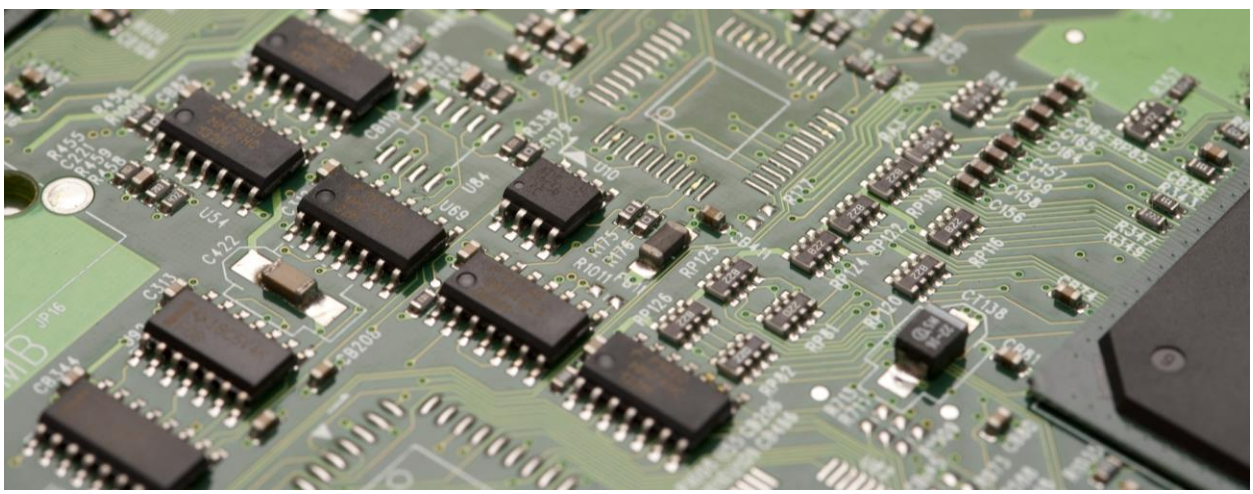
INTRODUCTION TO INTEGRATED CIRCUIT DESIGN

CHAPTER 1
INTRO TO INTEGRATED CIRCUIT DESIGN

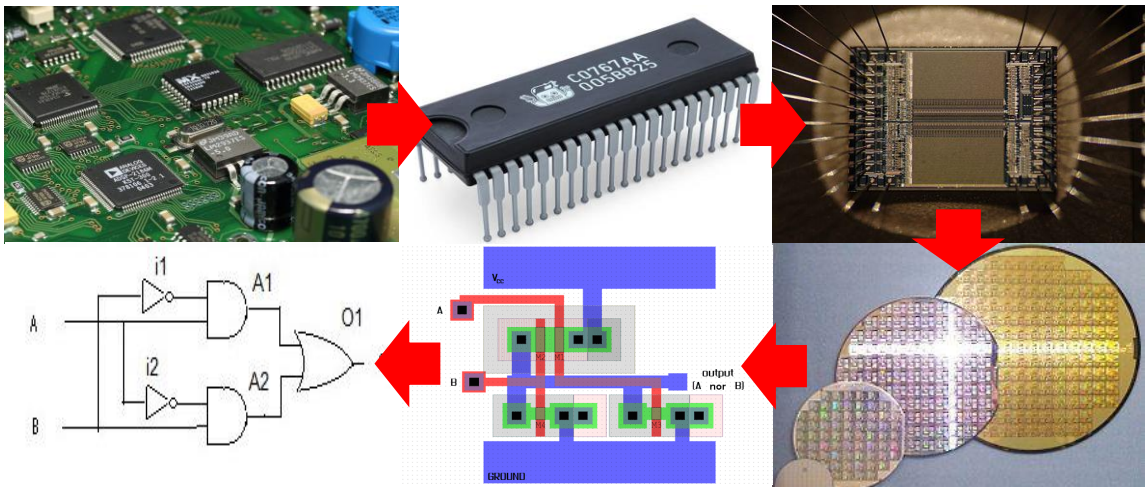
In 1958 IC's concept was first introduced. this concept has helped in the miniaturization of a lot of components like mobiles, computers, laptops, and many more devices in the digital world. It has reached great technological heights than any other concepts since then[1].

The invention of vacuum tubes has started the digital area. Vacuum based computers were rare and expensive at that time which then being replaced by faster and smaller in size transistors. It successfully reduce the cost, consume less power and more reliable. Then integrated circuits (IC) were invented which just revolutionized the use of computers. Even the common man is familiar with its applications like smart phones and laptops due to its small dimension, low cost, and very high reliability.



Definition of Integrated circuit – a group of complex set of smaller components and their interconnections that are fabricated (imprinted) onto a semiconductor material such as Silicon, GaAs etc. The size of the circuit can be as small as few square centimeters or only a few Square millimeters. While the individual circuit. components sized generally in micron and can be as small as nano in size. Integrated circuits are also known as ICs or chips. An ICs performs the same function as a larger circuit made from discrete components

INTRO TO INTEGRATED CIRCUIT DESIGN



History Of Semiconductor

The integrated circuits history start with the invention of the transistor in 1947 at the American Telephone and Telegraph Company's Bell Laboratories by William B. Shockley and his team. Shockley's team (including John Bardeen and Walter H. Brattain) found that, electrons would form a barrier at the surface of certain crystals under the right circumstances. By manipulating this barrier, they learned to control the flow of electricity through the crystal. Based on this knowledge the team created a device that could perform certain electrical operations, such as signal amplification, which were previously done by vacuum tubes. This device named as transistor. In 1958 Jack Kilby and Robert Noyce independently thought of a way to reduce circuit size further. They create a small wire by putting a very thin paths of metal (usually aluminum or copper) directly on the same piece of material. By using this technique Integrated circuit (IC) created, an entire circuit now possible to be integrated on a single piece of solid material.. The invention of the integrated circuit made technologies of the Information Age feasible rather than before. Vacuum tubes technologies unrealistically awkward and very expensive. ICs today are growing rapidly and are widely used in daily life, from cars to toasters to amusement park rides[1]

Application Of An ICs

Most of electronic devices consist of an ICs. The application of an ICs expanding from time to time. Due to its high reliability and compact size, ICs found its way in military applications, state of the art communication systems, and industrial applications. The shrinking ICs size allows millions of transistors and other discrete components to be embedded on it. ICs is basically a complex set of some discrete circuits on a small chip that is made of a semiconductor material like silicon can also be called a microchip.

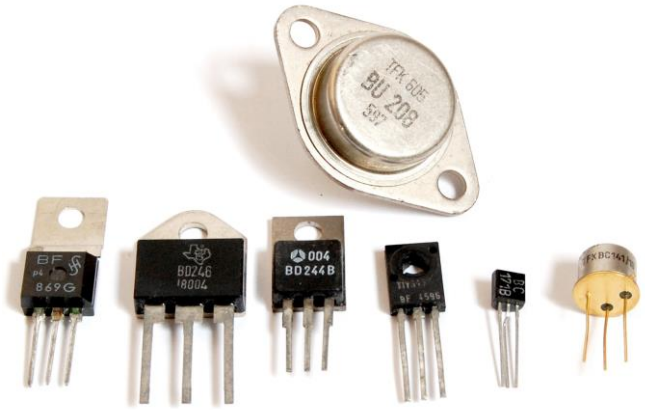
Most electronic equipment today use integrated circuit, for example:

I. Computer / Server / workstation
II. TV / Radio / Video
III. Cell Phones
IV. Digital Clock
V. Robotic Systems
VI. Telecommunication System
VII. Automotive
VIII. Medical Equipment
IX. Aerospace
X. Children's Toys
XI. Military Field
XII. etc.

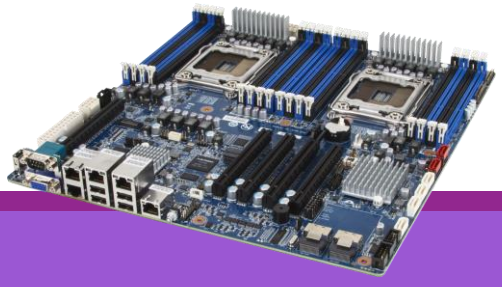
There are some factors that cause the replacement of discrete circuits with an ICs. Transistors, resistors, diodes, capacitors, and many other discrete devices consume more space. Depending to the need of circuitry, each of them is soldered on to printed circuit boards (PCB) which will then occupy a large space. Another drawback is reliability issue due to the use of many components. Thus challenged the engineer to design more reliable and smaller size microcircuits

Discrete Components

All the individual transistors, diodes, resistors, capacitors, and inductors were discrete in nature before the invention of integrated circuits (ICs). Either discrete components or an ICs can be used to construct a system. An IC made up of silicon wafers, all the components processed on the wafers to create an IC. One problem in ICs manufacturing is some of discrete circuits may not be possible to be created on a silicon wafer. The construction of discrete circuit consists of components that are separately manufactured. Conducted wires then used to connect all the components on a circuit board or printed circuit board (PCB). One of the primary components used in discrete circuit is transistor.



Definition of Discrete Components - Discrete components are opposed to integrated circuits (ICs), which include individual electronic components on a chip including resistors, capacitors, and diodes etc. it is constructed as a single unit elementary electronic device. All electronic components such as transistors, resistors, capacitors and diodes were discrete before the advent of integrated circuits (chips). Discrete components are widely used in amplifiers and other electronic products that use large amounts of current[2].



Advantages Of Integrated Circuits

1 Small in size

The IC becomes a lot smaller as fabrication process is used for the integration of active and passive components on to a silicon chip. It may be at least a thousand times smaller when compared to a discrete circuit.

2 Very low weight

When compared to the discrete circuit, the weight of the IC also reduces due to small size.

3 Low cost

The manufacturing of an ICs usually in mass production. the cost of production will be very low and less time consuming. Million of wafers are fabricated on a single wafer.

4 Low power consumption.

Lesser power consumption and lesser power loss due to smaller size of ICs.

5 High reliability.

Soldered joints on the PCB will make it less reliable. In ICs this problem is omitted. There is no soldered joints, with fewer interconnections, and thus highly reliable.

6 Easy replacement.

In a discrete circuitry, if any single component faulty, it will cause the whole circuit to fail. The faulty component has to be desoldered and replaced. Troubleshooting also very difficult to be done. This problem can be omitted in an IC by replacing an entire IC as it is low in cost.

ICs Packaging

IC packaging is very crucial to keep each semiconductor chips reliable over many years of use and protected from elements and possible stresses. IC packaging actually is a technology that being used to protect the circuit from corrosion or physical damage and allow mounting of the electrical contacts connecting it to the printed circuit board (PCB) which surrounds the circuit material. There are different types of IC packaging systems designs to consider due to many different types of integrated circuits available.

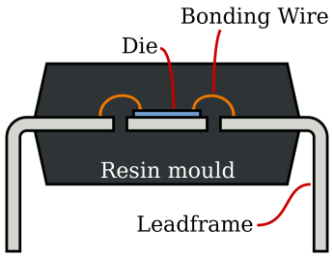
IC packaging designs are categorize based on formation and break into lead-frame type or the substrate type.

PLASTIC

- DIP - dual in-line package
- SIP - single in-line package
- TSOP - Thin small outline package
- QFP - Quad flat package
- PLCC - Plastic leaded chip carrier
- LCC - Leadless chip carrier

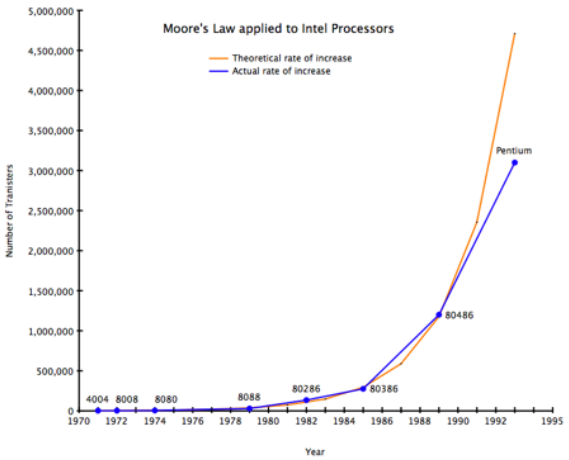
CERAMIC

- CERDIP
- pin grid array.



Moore's Law - Gordon E. Moore, the co-founder of Intel predicted that the number of transistors on a microchip doubles every two years. Speed and capability of the devices can be expected to increase also based on his perception. This growth is exponential.

- Small scale integration (SSI)—2 to 10 gates/chip
- Medium scale integration (MSI)—100 to 1000 gates/chip
- Large scale integration (LSI)—1000 to 20,000 gates/chip
- Very large scale integration (VLSI)—20,000 to 1,000,000 gates/chip



CHAPTER 2

INTEGRATED CIRCUIT FABRICATION PROCESS

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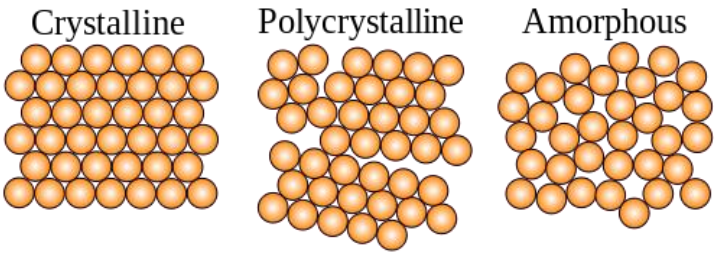
INTEGRATED CIRCUIT FABRICATION PROCESS

Crsytal Growth

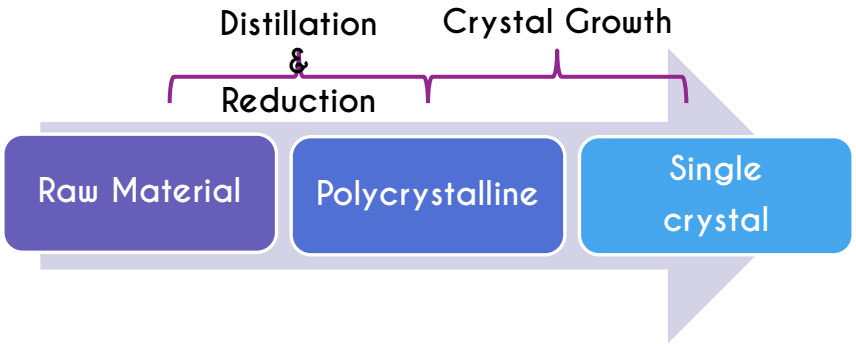
Types of Silicon Crystal Structure - Solid materials exist in the form of crystal and amorphous. Atoms are arranged periodically for solid crystal. Such material is defined as single crystal. polycrystal is formed if the atoms arranged in a few different single crystal structures.



Single Crystal - Atoms are arranged uniformly all over the material in single crystal structure. Single-crystal silicon substrates that possess a high level of purity and perfection is used to built Integrated Circuits. This type of structure does not have defects that have been known to limit the lifetimes of minority carriers. Material such as silicon must also have a high degree of crystalline perfection, a high degree of chemical purity and high structure uniformity apart from being single-crystalline in nature.

Polycrystalline - Material consisting of multiple small silicon crystals form a Polycrystalline silicon. This type of material (polysilicon) is used as the conducting gate material in MOSFET and CMOS processing technologies.

Amorphous - Materials in which the atoms and molecules are not organized in a definite lattice pattern is known as amorphous or non-crystalline solid. This structure lacks the long-range order characteristic of a crystal.



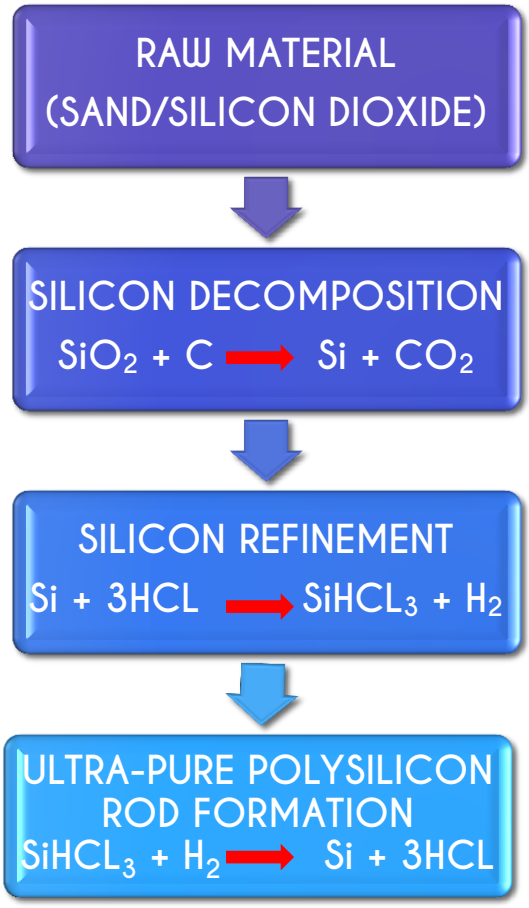
Crystalline Structure For IC Fabrication

INTEGRATED CIRCUIT FABRICATION PROCESS

Polysilicon Rod Preparation

Silicon wafer is used as starting material (substrate) for the fabrication of integrated circuits. The process of producing silicon wafer start with the Polysilicon rod preparation which then go through crystalline growth process to change the structure of a polycrystalline to single crystal.

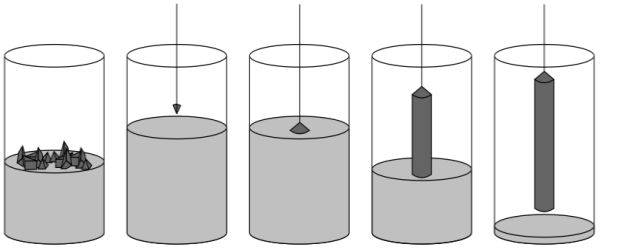
- One of commonly used raw material to produce wafer is silicon. Silicon is obtained from 99.99% pure sand heated in high temperature.
- Sand (silicon dioxide) is heated with carbon to get silicon through decomposition process.
- To refine silicon, hydrochloric acid is heated with silicon at 1000°C forming silicon trichlorosilane and releasing hydrogen gas.
- To get the ultra-pure silicon with 99.99999% pure, silicon trichlorosilane is heated with hydrogen at 1000°C[3]

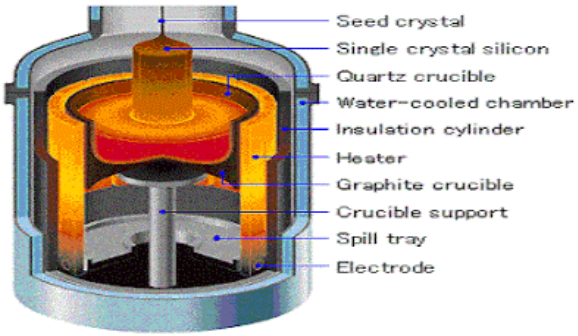


Single Crystal Growth

Single-crystal silicon substrates is used to build Integrated Circuits. Single crystal silicon obtained through a crystalline growth process which change the structure of a polycrystalline to single crystal. There are few methods that used to grow silicon crystalline ingot. We will discuss two commonly used methods, which are Czochralski and Float-zone methods.

Czochralski Process

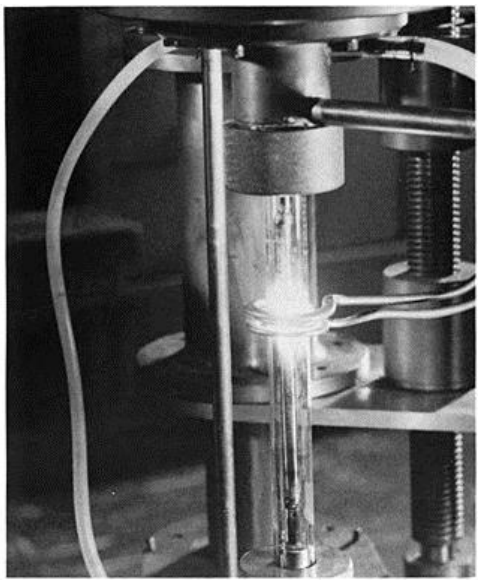




1. The polycrystalline silicon is melted in a quartz crucible nearly above the melting point of silicon. Dopants (e.g. boron or phosphorus) can be added to the melt to achieve appropriate electrical characteristics of the single crystal .
2. A seed crystal (a perfect single crystal) on a rotating rod is brought to the surface of the silicon melt.
3. In contact with the seed crystal, the melt overtakes its crystal structure.
4. The seed is slowly pulled upward with constant rotation, while there is constant contact with the melt.
5. The crucible turns in the opposite direction of the seed crystal.
6. A constant temperature of the melt is essential to ensure a steady growth.

Single Crystal Growth

Floating Zone Method

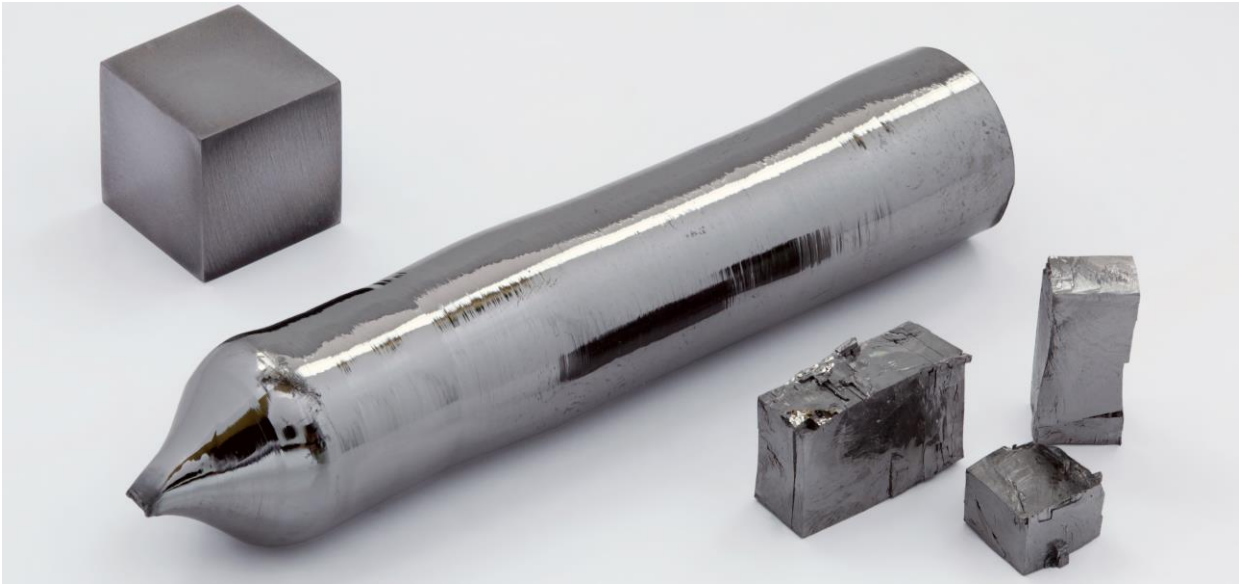


1. A seed crystal, which is introduced to the end of the polycrystalline silicon rod, sets the crystal structure.
2. The heated region is slowly guided along the rod, the polycrystalline silicon rod slowly transforms into a single crystal.
3. polycrystalline silicon is molten, it can hardly be polluted (impurities accumulate at the bottom since their higher solubility).
4. The doping is done by additions of dopants into the inert gas (e.g with diborane or phosphine) which flows around the apparatus.

Wafer Preparation

Wafer is use as a basic material in the fabrication of integrated circuits and other micro-devices. Wafer is a thin slice of semiconductor material such as a silicon crystal. The process for wafer preparation start with single crystal ingot formation through Czochralski and Floating Zone methods.

Wafer Preparation



Electronic grade Si (EGS) is the starting material for Si wafer manufacture. EGS is a Si ingot which can be shaped and cut into the final wafers. Impurity levels of EGS is very high with desired doping levels, So the chemical composition of the final Si wafers can be match.

Ingot Characteristics

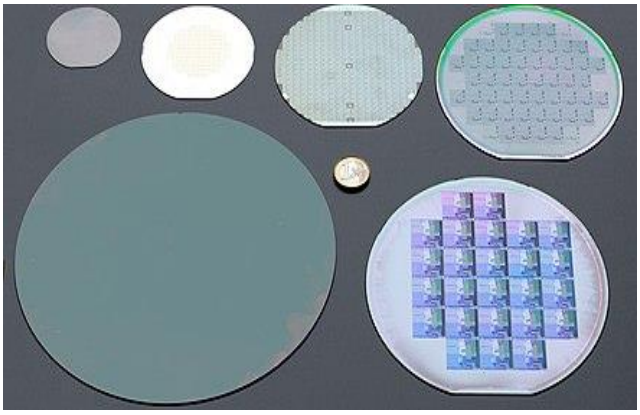
Czochralski	Floating Zone
The diameter of the single crystal is determined by the drawing speed, which provides 2 to 25 cm/h. The higher the drawing speed, the thinner the crystal.	Diameter is usually between 50-150 mm
Ingot diameter is between 100-200mm. Ingot with the diameter of 100mm can be grown up to 140cm long.	Ingot with the diameter of 110 mm can be grown up to 110cm long.
The material resistivity, ρ is between 0.01 to 50 Ω - cm.	The material resistivity, ρ is between 10 to 200 Ω - cm which is very suitable for power devices and sensors.

INTEGRATED CIRCUIT FABRICATION PROCESS

Wafer Preparation

Wafer Formation Process

1. Wafer fromation proces start with single crystal growth process (CZ or FZ), producing single crystal silicon ingot.
2. Silicon ingot is grinded to get uniform diameter according to the sizes.
3. Flats cut into one or more sides indicating the crystallographic planes of the wafer. Additional flats at different angles to show the doping type. Wafer orientation is identified through a single small notch made along the silicon ingot.
4. To form wafers, silicon ingot is sliced.
5. Wafer obtained is polished to smooth the uneven surface and smoothly planarized the surface to support optical photolithography.



SINGLE CRYSTAL GROWTH (CZ OR FZ)

↓

INGOT DIAMETER GRINDING

↓

FLATS AND NOTCHES SHAPED ALONG THE INGOT

↓

WAFER SLICING

↓

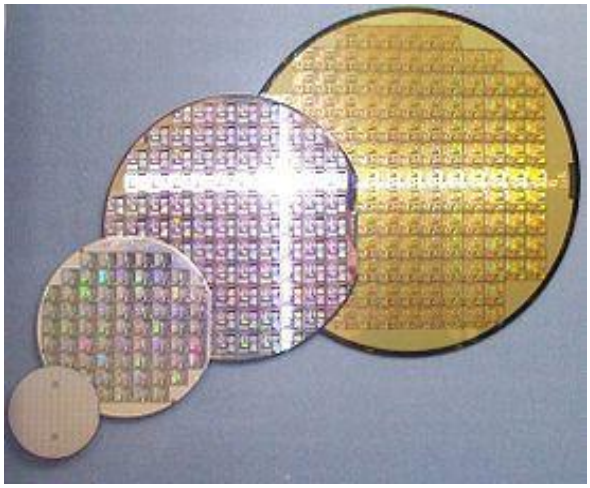
WAFER SURFACE POLISIHNG

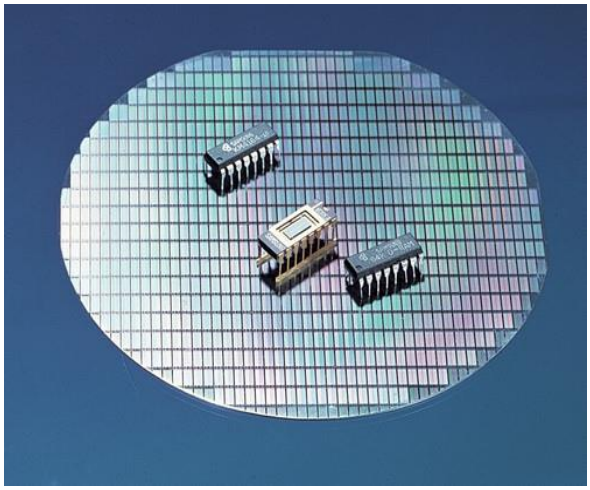
↓

WAFER IS READY FOR IC FOR IC PROCESSING

IC Fabrication Process

The manufacturing of Integrated Circuits (IC) is a mass production process which follow few basic steps. These steps including creation of 8-20 patterned layers into the substrate to form the complete integrated circuit. The electrically active regions are created due to this layering in and on the surface of wafer. On a single thin silicon, more than thousand even million of transistor can be made which then is cut into individual IC chips.





1st Step: Wafer Production

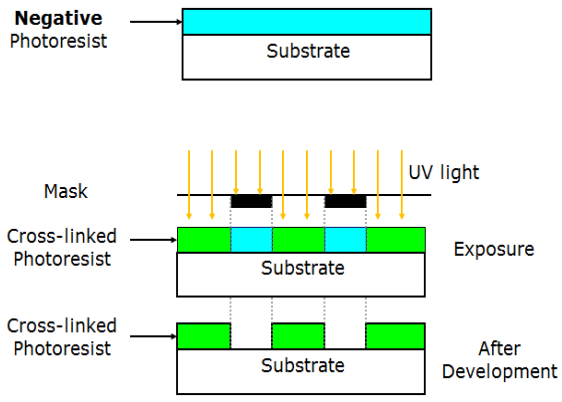
IC fabrication process start with wafer production which already explained in previous topics. Wafers is a slice of round semiconductor material that use as a substrate to manufacture IC, usually silicon. Silicon is widely used because, at higher temperatures silicon remains at its state compared to germanium and its second most abundant material in the earth crust. **Epitaxial growth** single silicon crystal is grown upon original silicon substrate to form a uniform layer of silicon dioxide on the surface of wafer.

2nd Step: Wafer Production

One of the most important process in fabrication is photolithography which used to protect some area of wafer when working on another area and transferring geometric shapes on a mask to the surface of a silicon wafer. This process

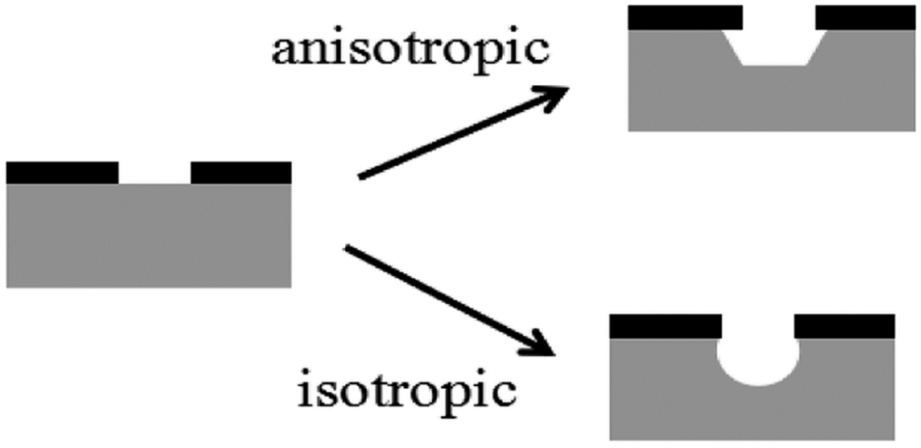
IC Fabrication Process

includes masking with a photographic mask and photo etching. Wafer surface is applied with photoresist film that is sensitive to the UV light. By using a photo aligner, the wafer is aligned to a mask which then exposed to ultraviolet light through mask. Photolithography is performed in a yellow room with extremely low levels of particulates.



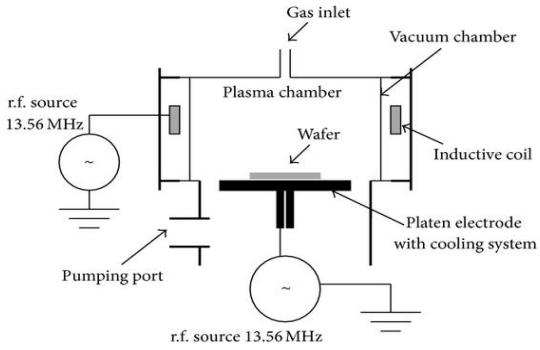
3rd Step: Etching

Etching is a process to remove selectively, material from the surface of wafer to create patterns. Etching mask used to protect parts of material. Commonly, there are two types of etching Either wet (chemical) or dry (physical) etching used to remove the unmasked material. Isotropic etching is used to perform etching in all directions at same time. Anisotropic etching is faster in one direction.



INTEGRATED CIRCUIT FABRICATION PROCESS

IC Fabrication Process



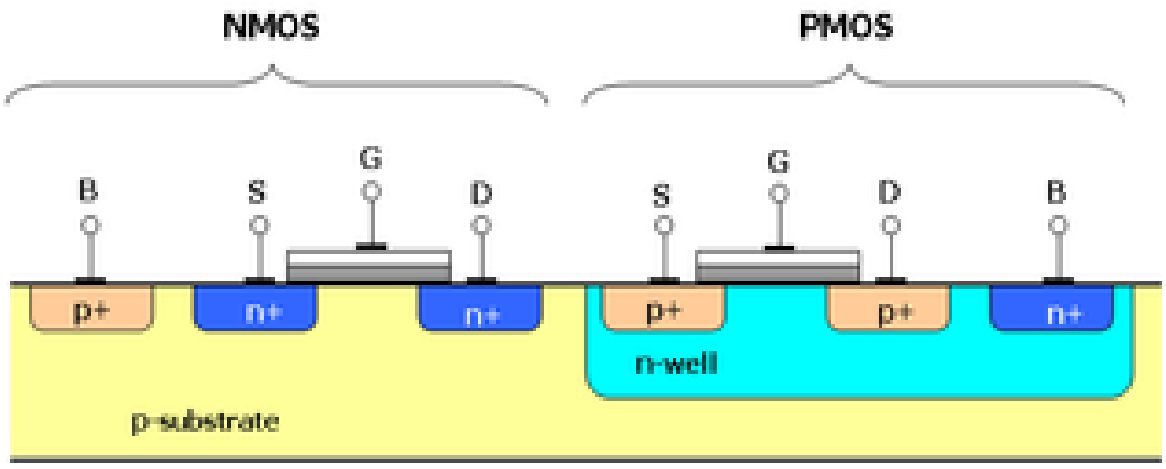
Wet etching is an isotropic process, mostly used in the manufacturing of circuits with feature sizes larger than 3 microns. Liquid chemical is used in wet etching and it is a highly selective with respect to mask and substrate. Dry etching in other hand is anisotropic process which remove materials uses gases. It usually used to define circuit features smaller than 3 microns. Dry etching is less sensitive compared to wet etching, the process parameters easily controlled (e.g., pressure, temperature, gas flow, power). The condition of the material after etching can be either normal, over etch and resist lifting or peel off.

	WET ETCHING	DRY ETCHING
METHOD	Chemical solutions	Plasma
ADVANTAGE	Low cost, easy to implement	Defining small feature size
	High etching rate	
	Good selectivity	
DISADVANTAGE	Inadequate for defining feature size < 1um	High cost, hard to implement
	Potential of chemical handling hazards	Low throughput
	Wafer contamination issues	Poor selectivity
		Potential radiation damage
DIRECTIONALITY	Isotropic	Anisotropic

IC Fabrication Process

4th Step: Doping

Doping process is used to change and increase the conductivity of semiconductor (silicon). Electrical characteristic of the silicon can be either P-type or N-type depending on the impurities atom that introduced to the pure silicon crystal structure. The modified semiconductor structure also known as extrinsic semiconductor. The N-type impurities atom known as donor and acceptor for the P-type. The impurities atom that suitable to be used are from group III (P-type) and V (N-type) in the periodic table. The function of doping layers are To control the silicon resistance and To conduct more current flow through n-type or p-type carriers available. Commonly methods to dope semiconductor are diffusion, ion implantation and epitaxy.



5th Step: Metallization

□ Metallization is a process to produce contact with silicon generate interconnection among components on chip. Thin layer of Aluminums metal deposited on wafer surface to establish these. Aluminum is common metal layer used due to its characteristic having a better conductivity, better mechanical bond with silicon, forms low resistance contact and it can be patterned with single deposition and etching process. The process such as masking, etching,

doping will be repeated for each successive layers until all integrated chips are completed. Silicon dioxide is used as insulator between the components on the device through a process called Chemical Vapor Deposition (CVD). Aluminium is deposited to create contact pads. For the protection over damage and contamination of the circuit, passivation layer deposited as a final dielectric layer. The individual IC then will undergo electrical functional testing to check the functionality of each chip on the wafer.

EXERCISES

IC Fabrication Process

1. Identify the differences between Small Scale Integration (SSI), Medium Scale Integration (MSI) and Large Scale Integration (LSI) in terms of number of transistors and their examples.
2. Explain etching process in IC fabrication.
3. Czochralski method is widely used in producing a single crystal silicon (ingot). With the aid of a diagram, explain THREE (3) steps to produce it.
4. Explain FOUR (4) methods to prevent latch-up problem in CMOS transistor operation.
5. State TWO(2) advantages of integrated circuit.
6. Differentiate between discrete devices and integrated circuits.
7. Wet or dry Oxidation are two methods used to produce oxide layer, known as silicon dioxide (SiO2). Explain briefly the Dry oxidation process in IC fabrication.
8. Integrated Circuit (IC) can be classified into THREE (3) categories. Explain the categories based on circuit function.
9. Phitolitography is the core process in integrated circuit manufacturing. Explain the differences between positives and negatives photoresist with the aid of diagram.
10. Referring to Figure A, state the wafer formation process from silicon ingot to silicon wafer in box A,B,C,D and E.

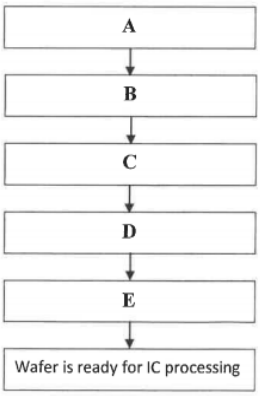


Figure A

CHAPTER 3

IC TESTING, YIELD AND RELIABILITY

CHAPTER 3

IC TESTING, YIELD AND RELIABILITY

The IC must first be electrically tested once its ready to ship for customer and ready to be used by the end users. Not all die on a wafer correctly operate. There are a lot possibility that can cause a device fail such as wafer fab-related defects, die cracked during assembly and the bonds were poorly connected or not connected at all. IC testing is a test procedure to identify good and bad die on the wafers thus isolate them. IC's chip testing comprises of different levels, it can occur at the wafer level, packaged-chip level, board level, system level and in the field. This procedure are very important. These procedures are very important because it is impossible to achieve 100% yield in IC's chips manufacturing. The manufactured IC's chips need to be screened of defects and failures before it is shipped out to the market. IC testing also need to be done to maintain the product quality and reliability.

IC Testing

Wafer testing is a step performed during semiconductor device fabrication. During this step, special test patterns apply to all individual integrated circuits that are present on the wafer for functional defects by using a piece of test equipment called a wafer prober. This test equipment can probe individual die (or sets of die) to determine circuit behaviors. wafer-level probing is performed to check CMOS integrated circuit functionality/ performance and final device parameters. Comparison between responses of vectors responses of vectors (patterns) from a good circuit with Device Under Test (DUT) is done. The circuit is good if the responses are the same or matches. Otherwise, the circuit is not manufactured as it was intended. inevitability, there will be some die will not pass all the vector sets which considered as fail die.[4]

IC TESTING, YIELD AND RELIABILITY

Final Testing

Upon completion of packaging sequence, individual IC must undergo a final test procedure. Before shipping of the final product to the customer final test is performed. This process is also known as product testing which includes electrical test and functional test. The test purposely to identify damaged during packaging if any and measure each device's performance characteristic.

Burn In

Burn-in is an electrical stress test to accelerate the electrical failure of a device by employing voltage and temperature. The electrical excitation applied during burn-in may mirror the worst-case bias that the device will be subjected to throughout its useable life which simulates the operating life of the device.

This test held in a temperature controlled burn-in "ovens" where the circuits are let to exercise at elevated voltages and temperatures for a few hours up to a few days. The reliability information obtained depending on the burn-in duration used which may pertain to the device's early life or its wear-out. Burn-in usually performed at temperature of 125 degree Celsius with application of electrical excitation to the samples.

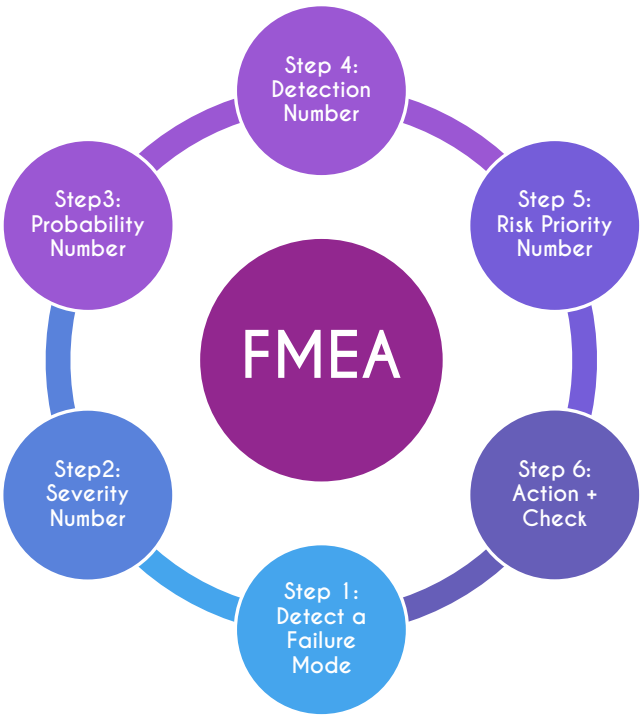
Reliability

The probability that a device will perform its required function, subjected to stated conditions, for a specific period is defined as product reliability. The reliability of a product can be predicted through a design-assist process obtaining the reliability characteristics of a system. In other words, it refers to techniques that can be used to predict reliability given a detailed description of a design.

One of commonly used technique for reliability prediction is **Failure Mode Effect Analysis (FMEA)**. It is a methodology designed to identify potential failure modes for a product or process. The risk associated with those failure modes assessed

and ranked the issues in terms of importance thus recognized any suitable corrective action to be carried out to address the most serious concerns. For easy understanding, just remember that FMEA is intended to document:

1. Its Failure
2. Its Mode
3. Its Effect
4. By Analysis



The process for conducting FMEA is summarized as follows:

- Describe product or process
- Define Functions
- Identify Potential Failure Modes
- Describes Effects of Failures
- Determine Causes
- Direction Methods or Current Controls
- Calculate Risks
- Take Action
- Assess Results

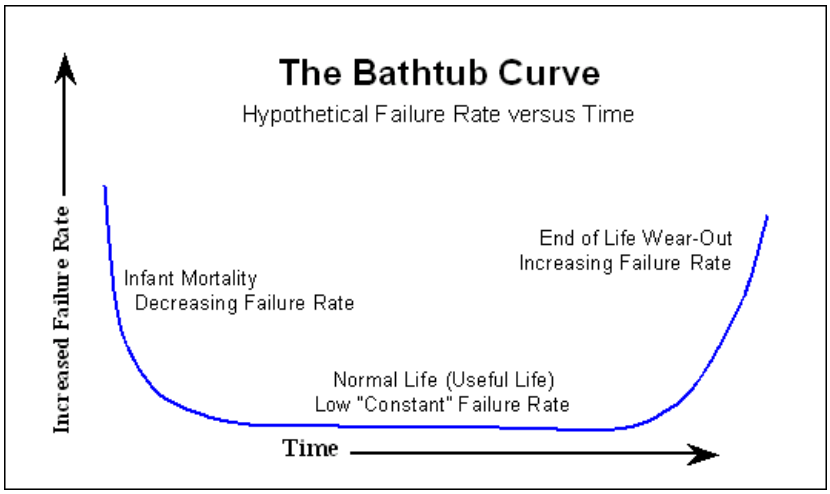
The potential problems identified through the analysis used some method to evaluate the risk associated with it. One of it is by using the Risk Priority Numbers (RPN):

RPN = Severity x Occurrence x Detection

The smaller the RPN – the better

and the larger the RPN – the worse

Bath-tub curve prediction of reliability



Reliability engineering widely used the **bathtub curve** that describes a particular form of the hazard function which comprises three parts which are infant Mortality, operating Life and wear out. Most products (as well as humans) exhibit failure characteristics.

Infant Mortality

The failure rate in the early life of a product is high but decreasing rapidly as defective products are identified and discarded including early sources of potential failure such as handling and installation error. To assure the integrity of design, technique such as burn in is used. All of these methods are designed to bring us to the useful life period before the customer sees the product.

Normal Life (Operating Life)

As the product matures, the failure rate becomes nearly constant where the weaker units fail and devices have entered the normal life period or operating life of the devices. During this period, failure rate relatively constant and this is the most common time frame for making reliability predictions.

Wear Out

As the time goes by, components begin to fatigue or wear out and failures rates increase. The cause of wear out in industrial electronic devices is due to the

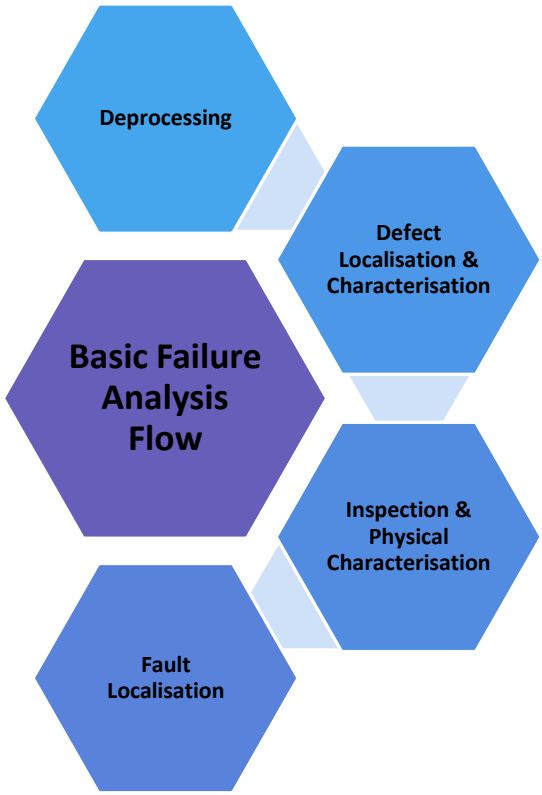
breakdown of electrical components that are subject to physical wear and electrical and thermal stress. Wear out should never occur during the useful life of a device, Industrial electronic devices are designed so that the useful life extends past the design life (when the device is obsolete).

Failure Analysis

Failure analysis is the process to collect data to determine the cause of a failure and analyzing it to further identified corrective actions or liability. Any non-conformance conformance of the product to its electrical and/or visual/mechanical specifications considered as a product failure. FA widely used to completely understand the cause of product failure and prevent it in the future.[5]

The techniques for FA fall into two categories:

1. **Non-Destructive**
   - ❖ No permanent effect on the part.
   - ❖ Allows subsequent testing for other failure mechanisms.
   - ❖ To be performed prior to destructive test (when components are still needed for further testing).
2. **Destructive**
   - ❖ Permanently change the device.
   - ❖ Does not allow for subsequent testing.
   - ❖ Perform when the cause of failure is known and to verify a hypothesis of the failure mode as obtained from the non-destructive tests.



EXERCISES

Designing Combinational Logic Circuit

1. Draw the symbol of PMOS and NMOS transistor.
2. Demonstrate the function of CMOS Inverter as a switch.
3. Illustrate the voltage transfer characteristic (VTC) of CMOS Inverter.
4. Define threshold voltage of NMOS transistor under static condition.
5. Illustrate CMOS inverter logic circuit by using NMOS and PMOS transistor.
6. Interpet Noise Margin (NM) equations from VTC CMOS Inverter.
7. Draw the cross section of PMOS transistor.
8. Sketch the switch of the static CMOS inverter when Vin=0 and Vin=Vdd.
9. Figure 9 shows a propagation delay curve of a real CMOS inverter. Referring to the curve, calculate the values of response time of the gate from low to high output transition (tpLH) and the propagation delay (tp).

CHAPTER 4

DESIGNING COMBINATIONAL LOGIC CIRCUITS

CHAPTER 4
DESIGNING COMBINATIONAL LOGIC CIRCUITS

4.1 Introduction

This chapter will present some basic characteristics and knowledge of CMOS families and combinational logic circuit design. The focus will be on combinational logic (or non-regenerative) circuits that have the property that at any point in time, the output of the circuit is related to its current input signals by some Boolean expression (assuming that the transients through the logic gates have settled). No intentional connection between outputs and inputs is present.

In another class of circuits, known as sequential or regenerative circuits, the output is not only a function of the current input data, but also of previous values of the input signals. This is accomplished by connecting one or more outputs intentionally back to some inputs. Consequently, the circuit "remembers" past events and has a sense of history. A sequential circuit includes a combinational logic portion and a module that holds the state. Example circuits are registers, counters, oscillators, and memory[6]. The differences between of combinational and sequential logic circuit are shown in the Figure 4.1 below.

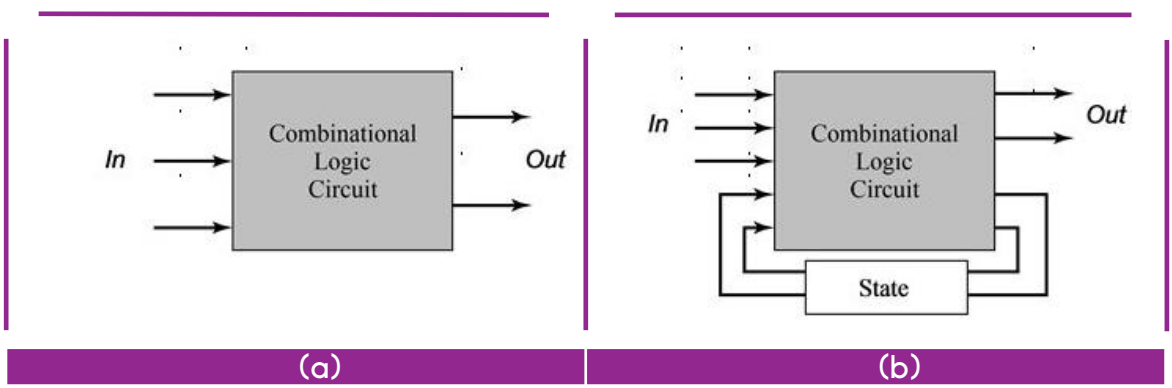


Figure 4.1 : Block diagram of (a) combinational and (b) sequential circuit logic[7]

4.2 NMOS and PMOS Transistor

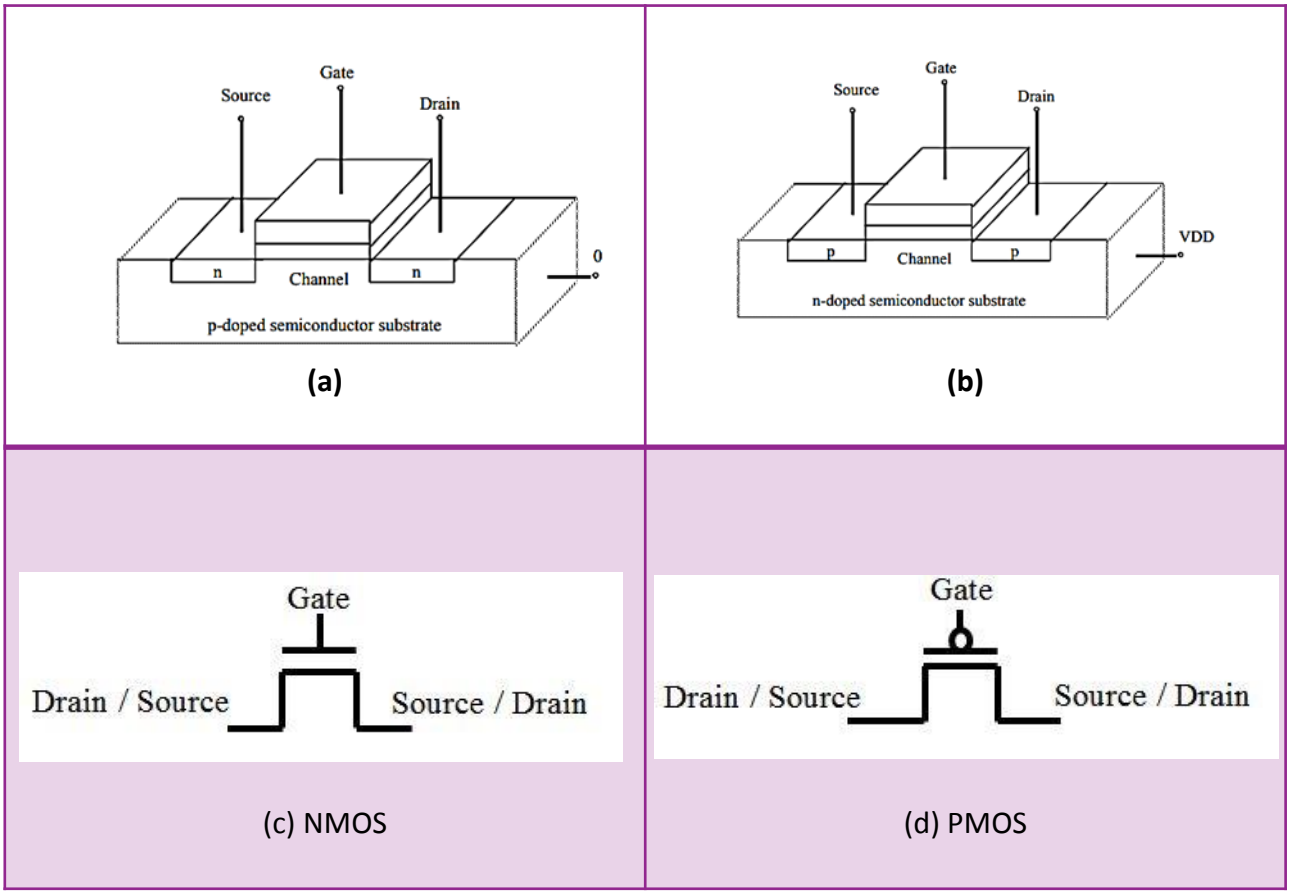


Figure 4.2 : The cross sectional view of a (a) NMOS transistor and (b) PMOS transistor with their symbol (c) and (d) [9].

Digital circuits for digital systems may be combinational or sequential. The sequential circuit will discuss in next chapters. Combinational circuits consist of a logic gates whose output at any time are determined directly from the present combination of inputs without regard to previous inputs. There is not requiring memory element. Sequential circuits, on the other hand, are circuits in which their outputs are dependent on not only the current inputs but also on past inputs. Because of their dependency on past inputs, sequential circuits must contain memory elements in order to remember the past input values. A digital circuit may contain both combinational circuits → and sequential circuits.[8].

DESIGNING COMBINATIONAL LOGIC CIRCUITS

4.3 Static CMOS Logic Circuits

Static memories preserve the state as long as the power is turned on. Static memories are built using positive feedback or regeneration, where the circuit topology consists of intentional connections between the output and the input of a combinational circuit. Memory based on positive feedback fall under the class of elements called multivibrator circuits. The bistable element, is its most popular representative, but other elements such as monostable and astable circuits are also frequently used.

CMOS logic circuit can be static or dynamic. Combinational logic (or non-regenerative) circuits have the feature that their output is connected to their current input signals by some Boolean expression at any point in time (assuming that the transients through the logic gates have settled).

Dynamic memories store state for a short period of time—on the order of milliseconds. They are based on the principle of temporary charge storage on parasitic capacitors associated with MOS devices. As with dynamic logic discussed earlier, the capacitors have to be refreshed periodically to annihilate charge leakage. Dynamic memories tend to simpler, resulting in significantly higher performance and lower power dissipation. They are most useful in data path circuits that require high performance levels and are periodically clocked[6].

4.3.1 Understand complementary CMOS circuit

The complementary CMOS design includes two networks: the pull-up network (PUN) and the pull-down network (PDN). Figure 4.3 depicts the development of the complementary CMOS circuit design using PUN and PDN. All the generic inputs are distributed to both PUN and PDN. The function of PUN is to provide a connection between the output and VDD anytime the output of the logic gate is meant to be 1 (HIGH). In the other hand, PDN functions to connect the output with GROUND when the output of the logic gate is meant to be 0 (LOW). The PUN and PDN networks are constructed in a way that one and only one of the networks is conducting the steady state. This is equivalent in stating that the output node is always a low-impedance node in steady state.

PDN is built with NMOS transistors, whereas PUN is built with PMOS transistors. In this case, the transistors' gate signal acts as a switch. When the P network is turned on, the output rises to the supply voltage Vdd, and when the N network is turned on, the output falls to Gnd[11]. The ultimate reason for using PMOS for PUN and NMOS for PDN is that NMOS generates 'strong zeros' while PMOS generates 'strong ones.' When NMOS devices are connected in series, a NAND gate function is implemented, and when they are connected in parallel, a NOR gate function is implemented. In contrast, PMOS devices connected in series impose a NOR gate, and those connected in parallel impose a NAND gate. As a result, a parallel connection of a transistor in PUN corresponds to a series connection in PDN[11]. The number of transistors needed for an N-input logic gate is 2N.

4.3 Static CMOS Logic Circuits

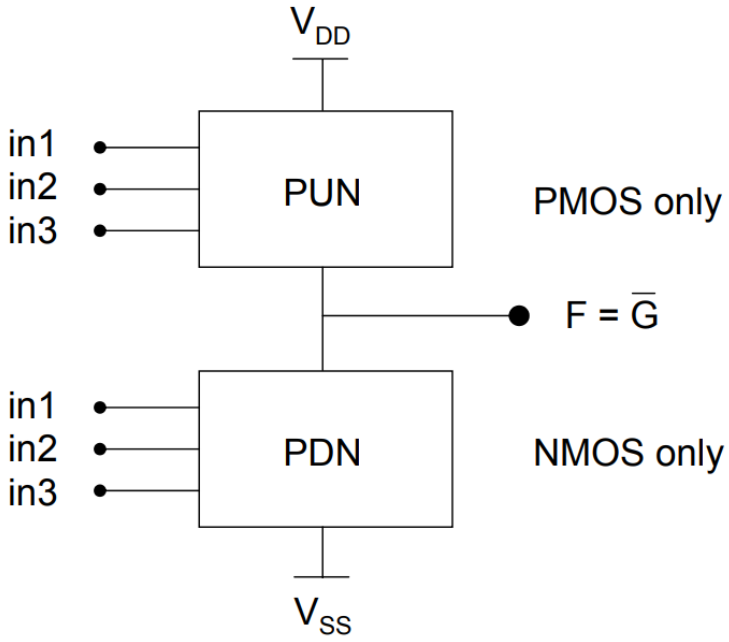


Figure 4.3 : Complementary Logic Gate as a Combination of a PUN (pull-up network) and a PDN (pull-down network)[7,10].

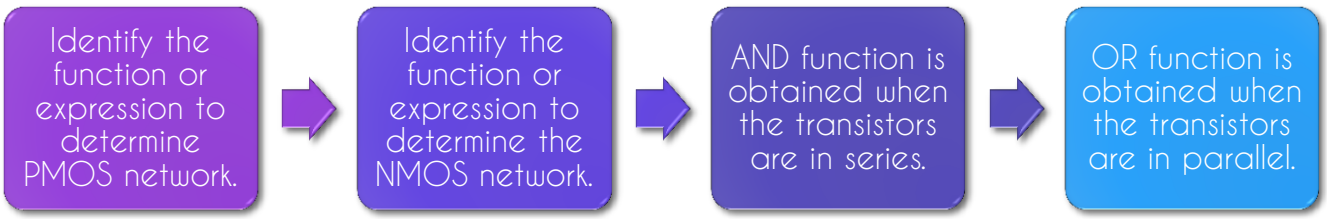
Comparison between complementary pull-up and pull-down network in a logic circuit.

Pull-up network	Pull-down network
pMOS transistor	nMOS transistor
serial connection	parallel connection
parallel connection	serial connection

DESIGNING COMBINATIONAL LOGIC CIRCUITS

4.3 Static CMOS Logic Circuits

The followings are the steps to construct complementary CMOS logic circuit:



Example of 2 and 4 inputs NAND gate with 2 and 4 inputs NOR gate is shown in Figure 4.4 below.

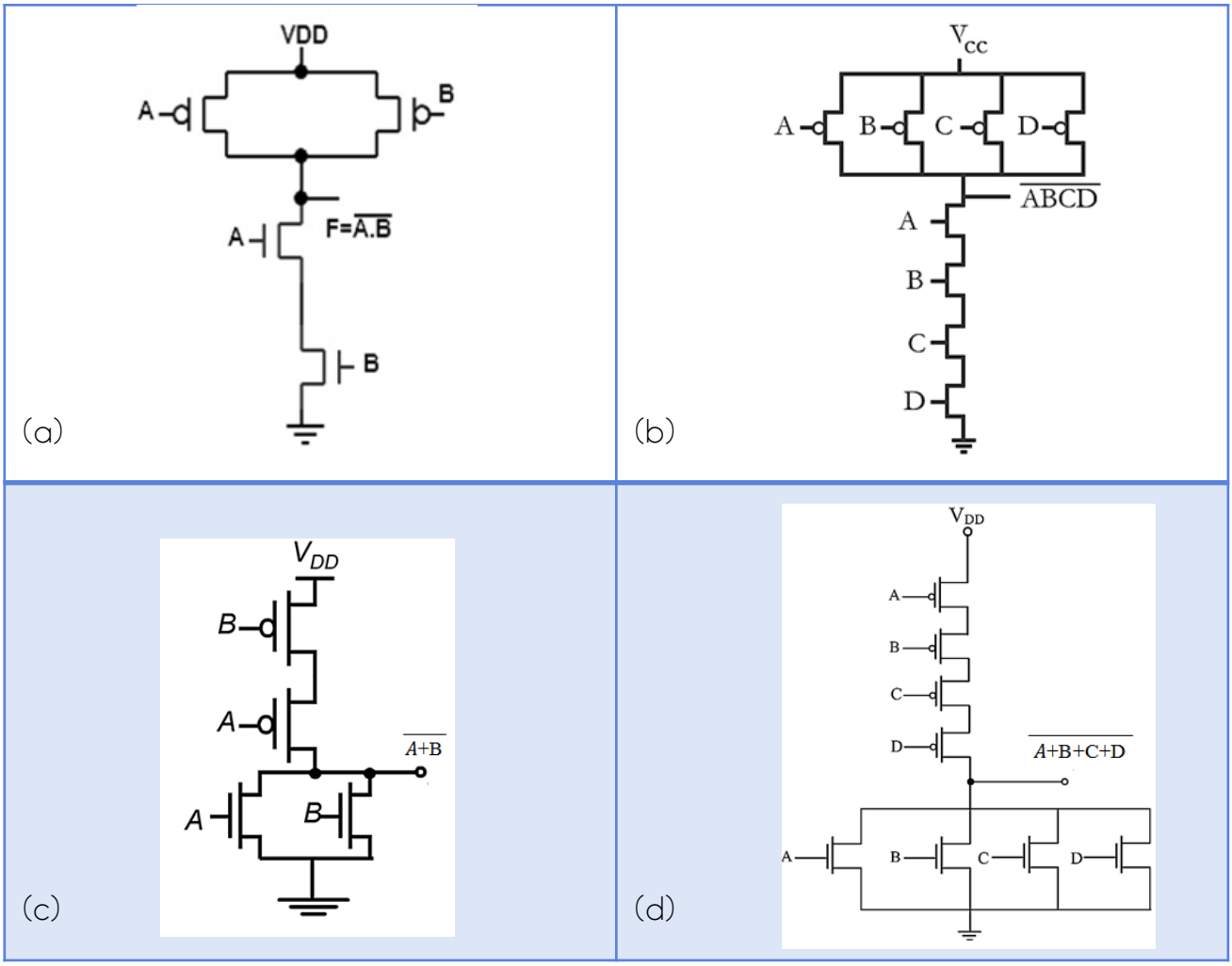


Figure 4.4 : The CMOS static logic gates: (a) 2 input NAND gate (b) 4 input NAND gate, (c) 2 input NOR gate and (d) 4 input NOR gate

4.3.2 Transistor Sizing

Transistor sizing is another important factor that must be considered in designing CMOS circuit as it affects the performance of the device in terms of propagation delay. It is ideal to have tPHL similar as tPLH. Assume the goal is to size a NOR gate such that it has approximately same delay time as a minimum sized inverter. Since the pull-down path in the worst case is a single device, the NMOS devices can have same width as the NMOS device in the inverter. For the output to be pulled high, both the transistors must be turned on. Since the resistances add, the device must be made two times larger compared to PMOS device in the inverter. Since PMOS devices have lower mobility compared to NMOS devices, stacking must be avoided as much CMOS IC DESIGN as possible[12]. Figure 4.5 shows the example of transistor sizing for logic gates

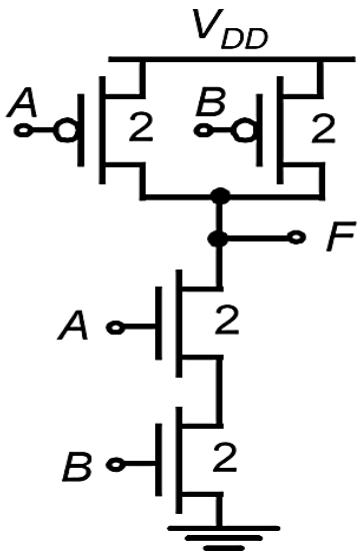


Figure 4.5 shows the example of transistor sizing for logic gates (NAND)

4.4 Ratioed logic

Ratioed logic attempts to reduce the number of transistors required to implement a given logic function at the risk of decreased reliability and increased power dissipation. When the PDN is turned off, the PUN in complementary CMOS acts as a conditional route between VDD and the output. The entire PUN is replaced in ratioed logic by a single unconditional load device that pulls up the output for a high output.

An NMOS pull-down network realises the logic function, and a simple load device are used instead of a combination of active pull-down and pull-up networks. Hence, Pseudo NMOS logic is a ratioed logic. Pseudo—NMOS logic uses only one PMOS device as a pull-up device for a multi-transistor N—Logic block. Thus, the required number of transistors for an N-input gate is an N+1 transistor.

The circuit diagram of a general ratioed logic, Pseudo-NMOS inverter, NAND and NOR gates is shown in Figure 4.6 below. Pseudo-NMOS logic outperforms static CMOS logic in terms of speed, especially in big fan-in NOR gates. This is because the output rise time is influenced by only one PMOS transistor[6].

The pseudo nMOS design technique saves dynamic power (by reducing capacitive loading) at the cost of non-zero static power by replacing a single pMOS transistor with its gate terminal grounded for the pull up network[13].

4.4 Ratioed logic

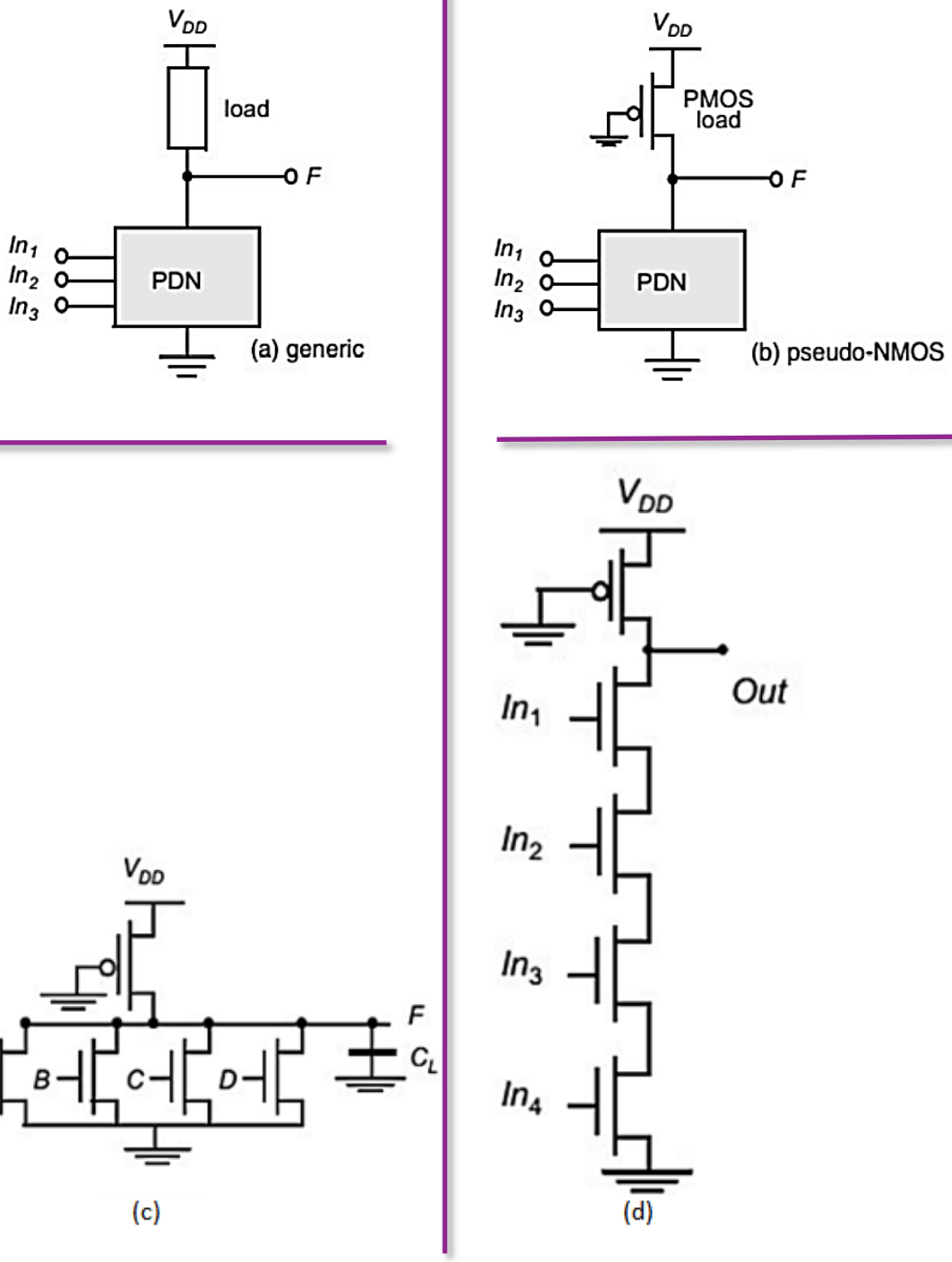


Figure 4.6 : The ratioed logic: (a) general (b) pseudo-NMOS, (c) 4 input pseudo-NMOS NOR gates and (d) 4 input pseudo-NMOS NAND gates

4.5 Pass Transistor logic (PTL)

Pass transistor logic is a popular and widely used alternative to complementary CMOS (PTL). To implement various logic functions, PTL employs pass transistors to directly pass logic levels from inputs to outputs. In comparison to static CMOS design, PTL implements the same logic level with far fewer transistors and therefore has lower physical capacitance. As a result, it takes up less space and consumes less energy. PTL has found widespread application in low-power VLSI design, quantum computing, nano-electronics, and optical computing[14].

Figure 4.7 depicts an NMOS transistor-based transistor-level implementation of the AND function. If the B input is high, the top transistor in this gate is turned on and the input A is copied to the output F. When input B is low, the bottom pass transistor is activated and passes a 0 signal. At first glance, it appears that the switch controlled by B is redundant. Its presence is required to ensure that a low-impedance path to the supply rails exists under all conditions, or in this case, when B is low.

However, an NMOS device is good at passing a 0 but not so good at pulling a node to VDD. Pass transistors are utilised in pass transistor logic to transmit high and low voltages. As a result, when the pass transistor pulls a node high, the output only charges up to VDD -VTn. In fact, the situation is exacerbated by the fact that the devices experience body effect because there is a tremendous source to body voltage when pulling high because the body is tied to GND and the source charge up close to VDD.[10].

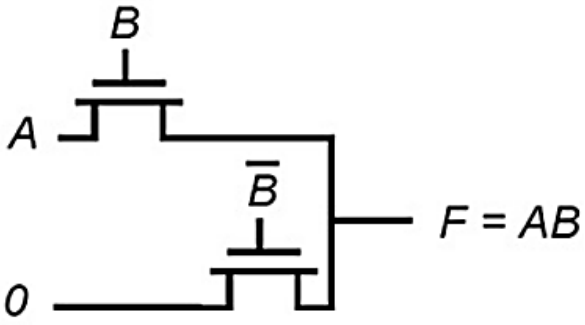


Figure 4.7 : Pass Transistor Implementation of an AND gate[10]

4.6 Dynamic CMOS in designing logic gates

Dynamic logic circuits offer numerous substantial advantages over static logic circuits in high density, high performance digital implementations where circuit delay and silicon area reduction is a fundamental goal. All dynamic logic gates rely on the temporary storage of charge in parasitic capacitance to function[11]. Dynamic logic is an alternative logic approach that achieves a comparable outcome while avoiding static power use. It uses a precharge and conditional evaluation phase sequence with the addition of a clock input.

Figure 4.8 shows the basic construction architecture of a (n-type) dynamic logic gate. The PDN (pull-down network) is built in the same way that complementary CMOS is. The precharge and evaluation stages of this circuit's functioning are separated by the clock signal CLK, which determines the mode of operation.

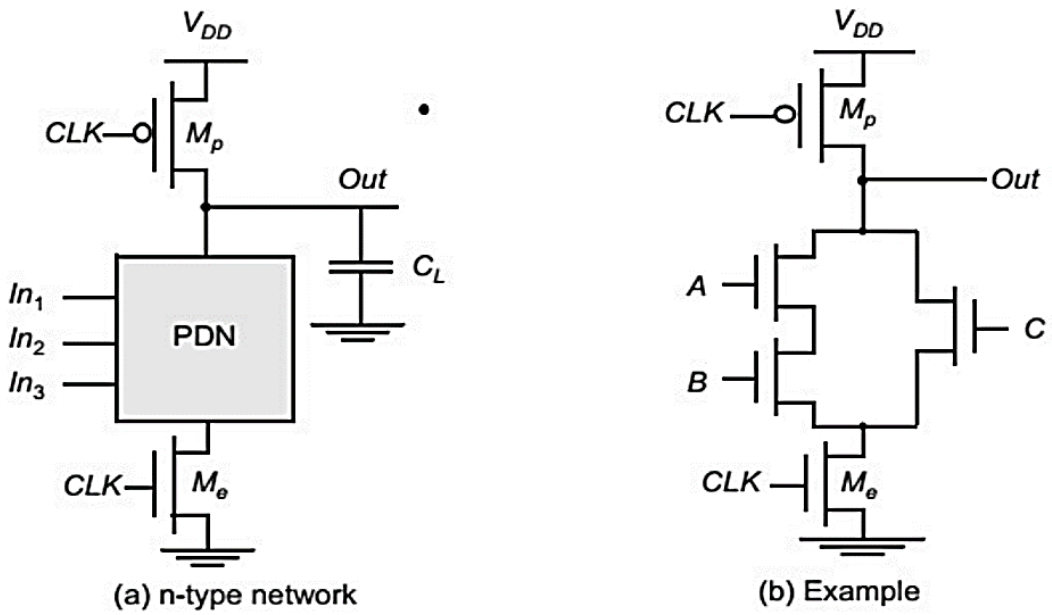


Figure 4.8 : Basic construction of dynamic gate

EXERCISES

Designing Combinational Logic Circuit

1. Draw the symbol of PMOS and NMOS transistor.
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3. Illustrate the voltage transfer characteristic (VTC) of CMOS Inverter.
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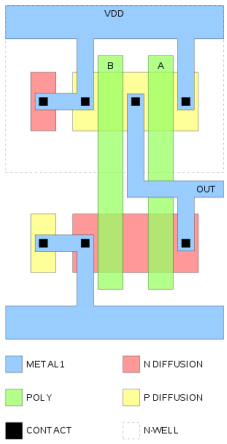
CHAPTER 5

LAYOUT DESIGN

LAYOUT DESIGN

5.1 Introduction to IC Layout

The backend design cycle is referred to as IC layout. As processes become more complex in VLSI design, the designer must understand the intricacies of the fabrication process and its relationship to IC layout. The design of each layer in photolithography is done with a CAD tool called a layout editor, which is a graphics package in which different material patterns are represented on the screen by different colours.



5.1.1 IC Layout Definition

Integrated circuit layout, also known IC layout, IC mask layout, or mask design, is the representation of an integrated circuit in terms of planar geometric shapes which correspond to the patterns of metal, oxide, or semiconductor layers that make up the components of the integrated circuit[15,16].

5.1.2 IC Layout Function

The following is the purpose of layout design of an IC:

To determine the number of connection layers and floor plans of the components or layers on the wafer according to the prescribed rules.

To produce the patterns of the masks needed for integrated circuit fabrication process.

5.1.3 Type of Layout

There are two types of layout which are stick diagram and actual layout which can be seen in Figure 5.1 below. IC layouts are created according to design rule specifications that are specific to a fabrication process. The layout editor is the designer's most important tool, and it's used to create a physical representation of a design based on a circuit topology. The stick diagram was introduced to address these and other shortcomings in the implementation of the layout design process, making the designer's job easier. The stick diagram allows a design engineer to visualize cell routing and transistor placement in a layout[17].

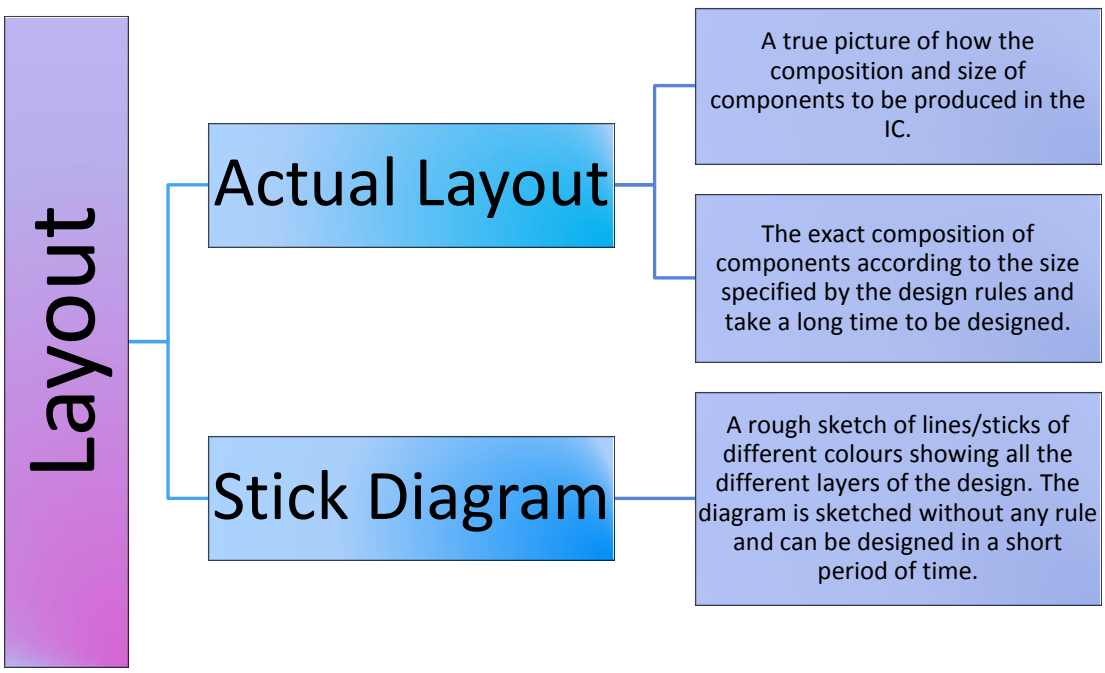


Figure 5.1 : Type of layout

5.1.3.1 Stick Diagram vs Actual layout

Stick Diagram vs Actual layout IC layouts are created according to design rule specifications that are specific to a fabrication process. The layout editor is the designer's most important tool, and it's used to create a physical representation of a design based on a circuit topology.

The stick diagram allows a design engineer to visualize cell routing and transistor placement in a layout[17]. Table 5.1 below shows the notations of the stick diagram.

Table 5.1 : The stick diagram notations

Colour	Stick encoding	Layers
Blue		Metal 1
Purple or Grey		Metal 2
Red		Polysilicon
Green		N – diffusion
Brown		P – diffusion
Black		Contact
Black		Via

5.1.3.1 Stick Diagram vs Actual layout

Stick Diagrams' Rules[18]

When two or more 'sticks' of the same type cross or touch each other that represents electrical contact.

When two or more 'sticks' of different type cross or touch each other there is no electrical contact. (If electrical contact is needed we have to show the connection explicitly).

When a poly crosses diffusion it represents a transistor.

In CMOS a demarcation line is drawn to avoid touching of p-diff with n-diff. All pMOS must lie on one side of the line and all nMOS will have to be on the other side.

5.1.3.1 Stick Diagram vs Actual layout

Figure 5.2 below shows the example of schematic, stick diagram and layout of CMOS inverter.

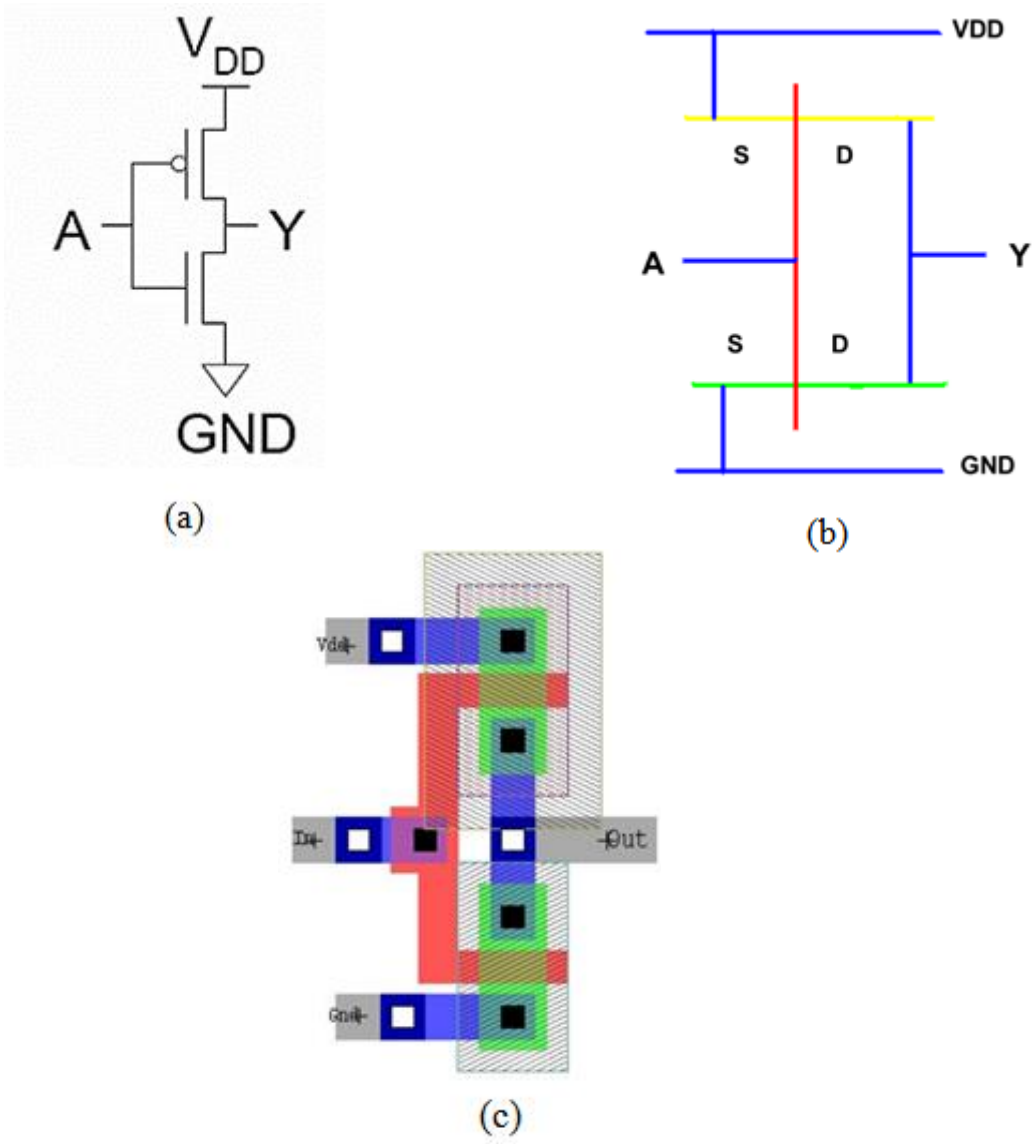


Figure 5.2 : Example of (a) schematic, (b) stick digram and (c) layout of CMOS inverter

5.1.4 Design Rule

A set of geometric boundaries known as layout design rules must be followed by the physical mask layout of every circuit to be fabricated using a specific process. On-chip line widths, component size, and separation are all specified in these standards.

The goal of the design rule is to obtain a high overall yield with dependability for each circuit made using a specific process on the smallest silicon chip possible[16]. Two units are being used which are scalable design rules (λ parameter) and absolute dimensions (micron rules) which can be seen in Figure 5.3.

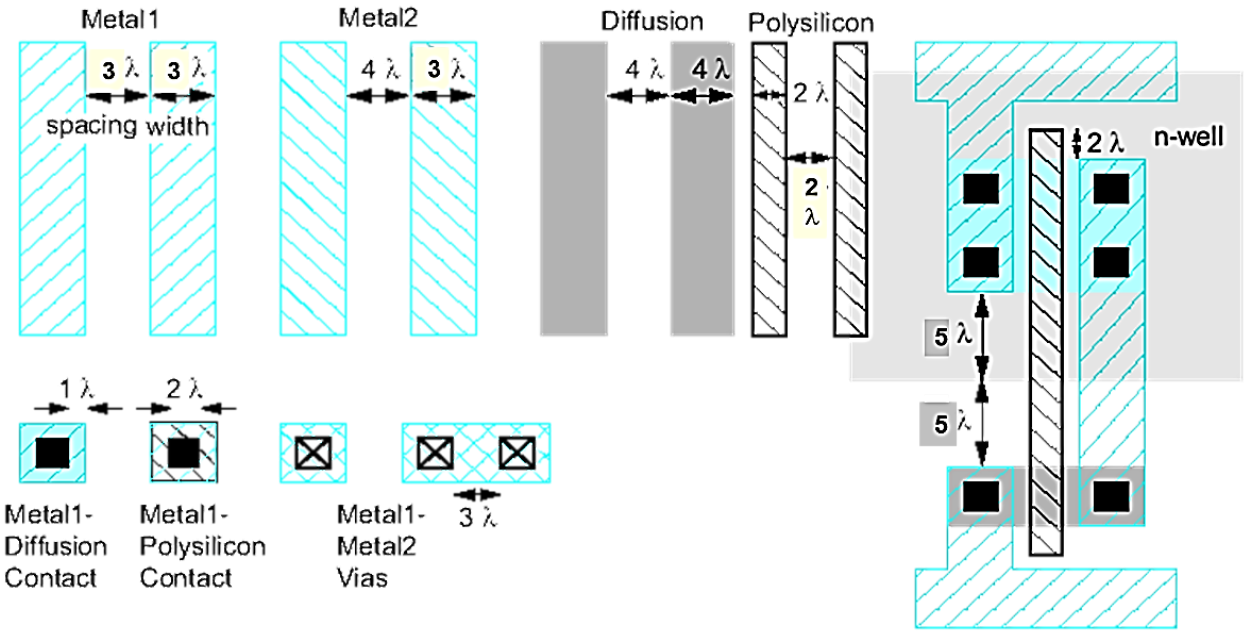


Figure 5.3 : Example of layout design rules in lambda

5.1.4 Design Rule

Table 5.2 shows the lambda-based layout design rules.

Table 5.2 : The lambda-based layout design rules feature[19]

Feature Name	Symbol	λ-Rule
Minimum active area (NSELECT or PSELECT) width	F1	3 λ
Minimum active area spacing	F2	3 λ
Minimum poly width	F3	2 λ
Minimum poly spacing	F4	2 λ
Minimum gate extension of poly over active area	F5	2 λ
Minimum poly-active edge spacing (outside active area)	F6	1 λ
Minimum poly-active edge spacing (inside active area)	F7	3 λ
Minimum metal spacing	F8	3 λ
Minimum metal width	F9	3 λ
Poly silicon contact width	F10	2 λ
Minimum poly contact spacing	F11	2 λ
Minimum poly contact to poly edge spacing	F12	1 λ
Minimum poly contact to metal edge spacing	F13	1 λ
Minimum poly contact to active edge spacing	F14	3 λ
Minimum active contact size	F15	2 λ
Minimum active contact spacing	F16	2 λ
Minimum active contact to active edge spacing	F17	1 λ
Minimum active contact to metal edge spacing	F18	3 λ
Minimum active contact to poly edge spacing	F19	3 λ
Minimum active contact spacing (on different active regions)	F20	6 λ

EXERCISES

Logic Devices

1. List the steps to construct a CMOS static circuit for 2 - input NAND gate.
2. List FIVE (5) differences between a combination logic circuit and sequential logic circuit.
3. Demonstrate the operation of AND pass-transistor logic.
4. Draw a CMOS static circuit for the Boolean function as shown below:-

$$F = \overline{(D + A \cdot (B + C))}$$

5. Draw pseudo-NMOS logic circuit for a 4-input NAND and a 4-input NOR gate.
6. Interpret the charge leakage for signal integrity issues in a dynamic CMOS design.
7. Sketch the block diagrams of a combinational logic circuit and sequential logic circuit.
8. Draw the construction of pull-up network (PUN) of NOR gate using only NMOS transistors.

CHAPTER 6

IC DESIGN METHODOLOGY

IC DESIGN METHODOLOGY

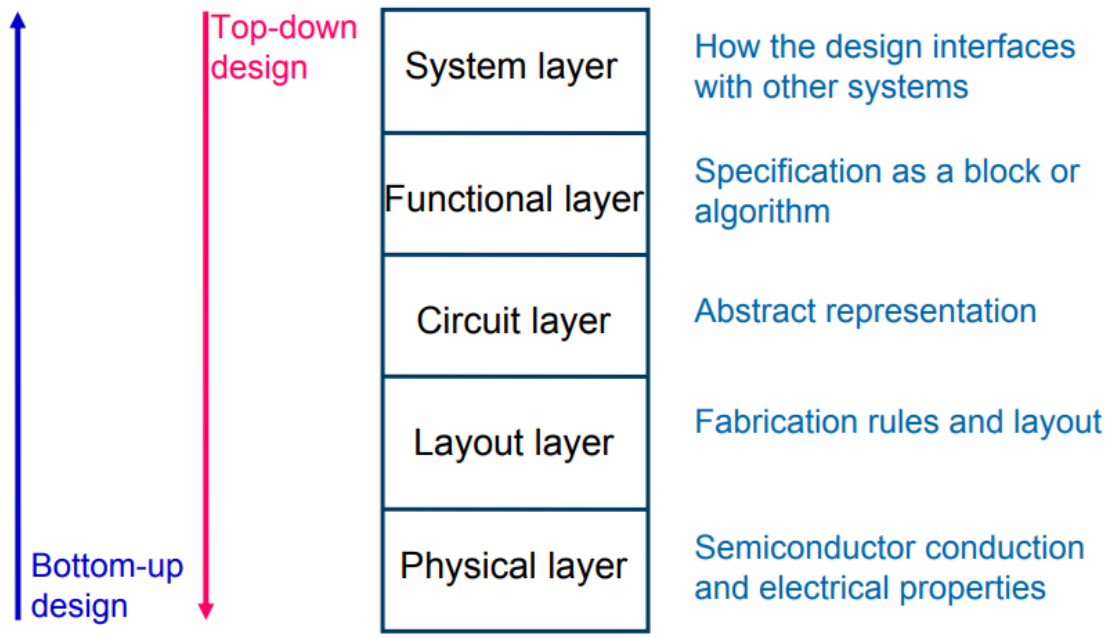
6.1 Hierarchy Design

Hierarchy design is a method of splitting a module into sub-modules and then repeating the process on the sub-modules until the smaller sections' complexity is manageable.

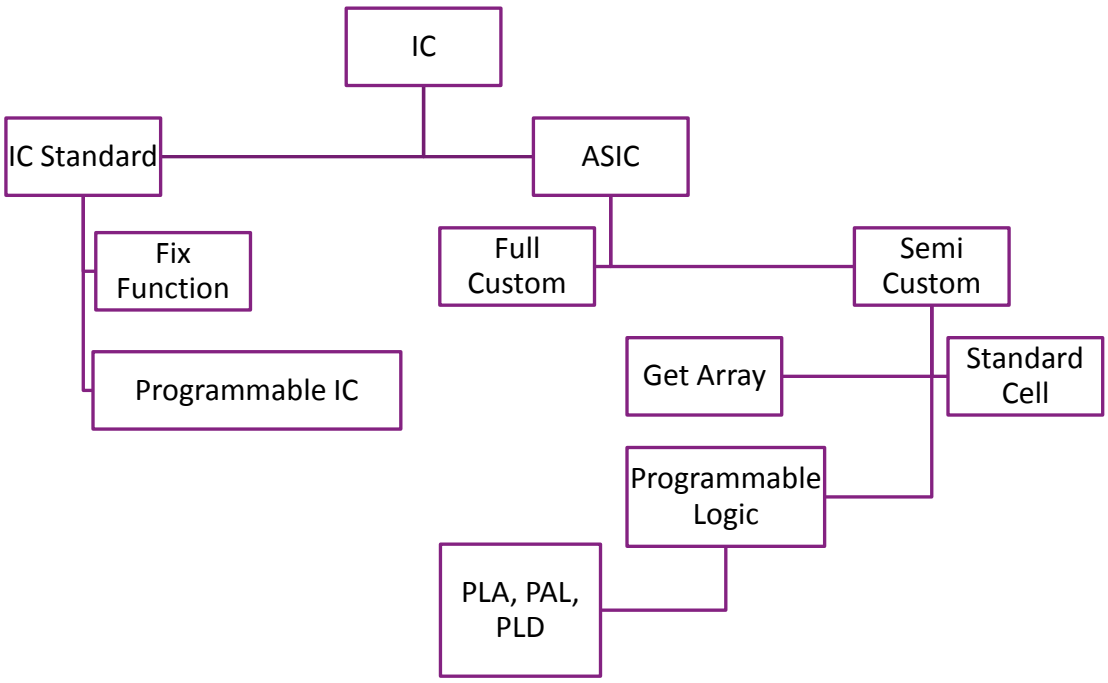
By separating the main system into multiple sub-modules, the hierarchical design technique decreases design complexity. At the end of the design phase, all of the blocks in the sub-modules can be easily combined to create the large system.

6.2 Design Methodology

The are two types of design methodology which is bottom-up and top-down method.



6.2 Design Methodology



Design Methodology Tree Diagram

Standard IC

In standard IC, integrated circuits designed and fabricated for general purpose used. IC is available in the market at a very low cost. Examples of standard Ics are 74 - SERIES TTL, 4000 - SERIES CMOS, OP-AMP, TIMER, INSTRUMENTATION AMPLIFIER, MEMORY, MICROCONTROLLER, etc.

ASICs :Application Specific Integrated Circuits

Definition : An integrated circuit (IC) customized for a particular use, rather than intended for general-purpose use. For example, a chip designed solely to run a cell phone is an ASIC.

6.2 Design Methodology

Full-custom IC Design

Full-custom IC design is a methodology for designing integrated circuits by specifying the layout of each individual transistor and the interconnections between them. • Full-custom IC design potentially maximizes the performance of the chip, and minimizes its area, but is extremely labor-intensive to implement.

Semi-custom IC Design

Semi-custom IC design is a methodology for making an integrated circuit which a portion of the circuit function is predefined and unalterable, while other portions can be configured to meet the designer's specific needs. There are 3 types of semi-custom design :

i. Gate array

ii. Standard cell

iii. Programmable Logic Device (PLD)

Design Styles	Advantages	Disadvantages
Full-custom	- Compact designs; - Improved electrical characteristics;	- Very time consuming; - More error prone;
Semi-custom	-Well-tested standard cells which can be shared between users; -Good for bottom-up design;	-Can be time consuming to built-up standard cells; -Expensive in the short term but cheaper in long-term costs;
Gate array	-Fast implementation; - Easy updates; -Only two layers of metal require customization;	-Can be wasteful of space and pin connections; -Relatively expensive in large volumes;

6.3 Programmable Logic Devices

Definition : PLD is an array of logic gates that can be programmed by the user which contains functions of a small number of logic circuits in a single chip.

PLD

PLD is an IC, designed to be configured by the customer or designer after manufacturing—hence "programmable".

The PLD configuration is specified using a hardware description language (HDL), similar to that used for an application-specific integrated circuit (ASIC).

PLD's consists of configurable logic blocks and flip-flops linked together with programmable interconnect.

Hierarchy of programmable interconnect allows the blocks to be "wired together"— somewhat like a one-chip programmable breadboard.

PLDs can be used to implement any logical function that an ASIC could perform.

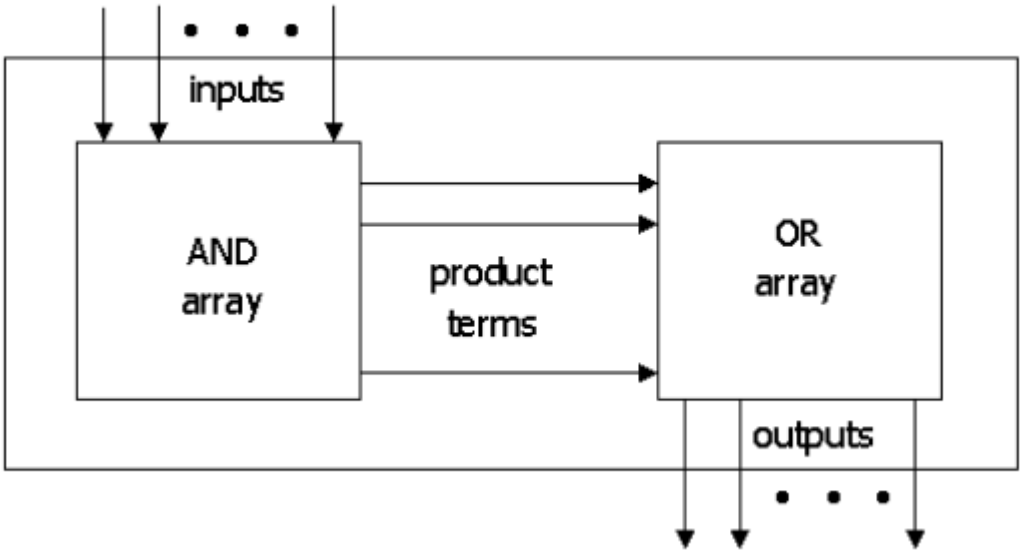
Advantages:

- Less time to market.
- The ability to update the functionality after shipping.
- Partial re-configuration of the portion of the design.
- The low non-recurring engineering costs relative to an ASIC design.

Disadvantages:

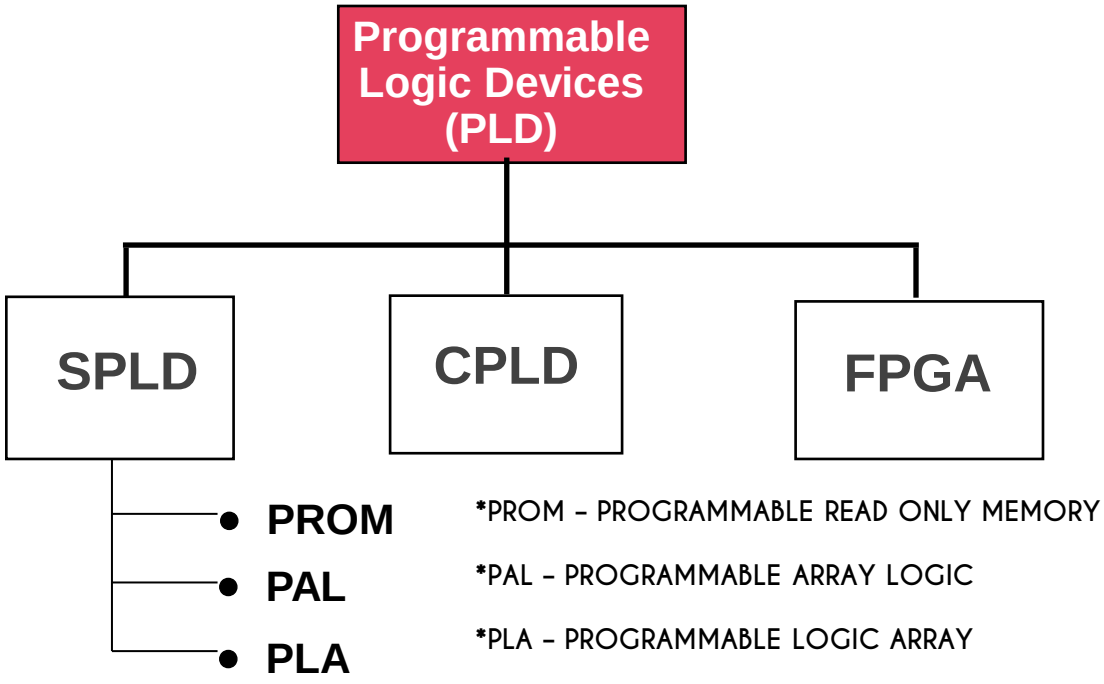
- Overall- performance is satisfactory, but not excellent if compared to ASICs.
- Requires more area

6.3 Programmable Logic Devices



Block Diagram of PLD Logic

There are three types of PLD Logic which are SPLD – SIMPLE PROGRAMMABLE LOGIC DEVICE, FPGA – FIELD PROGRAMMABLE GATE ARRAY and CPLD – COMPLEX PROGRAMMABLE LOGIC DEVICES



Types of PLD Logic

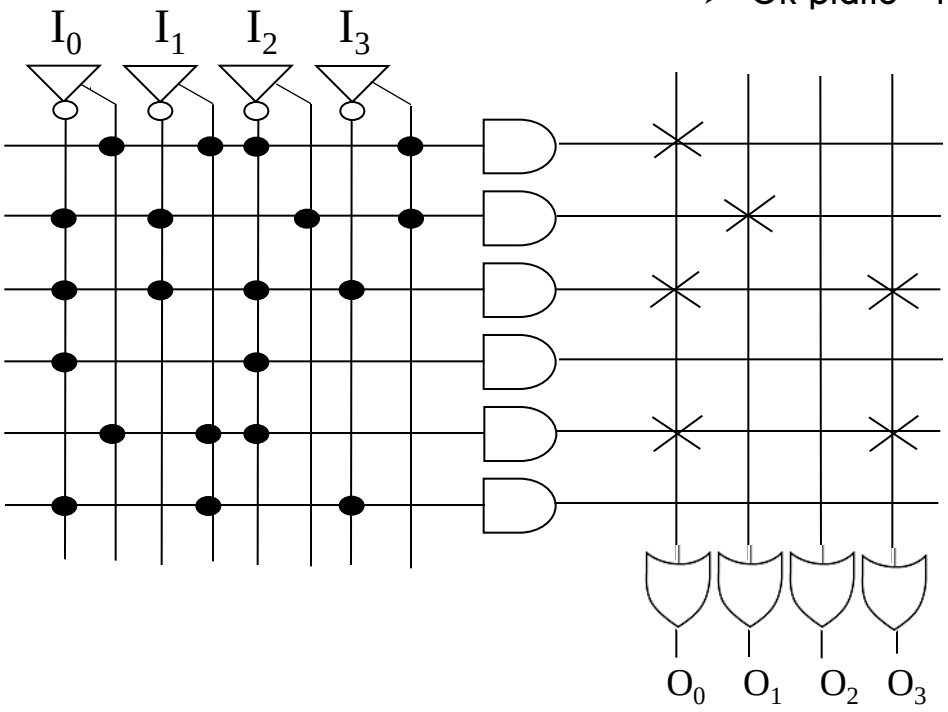
6.3 Programmable Logic Devices

PROM ARCHITECTURE

● = fixed by manufacturer

× = programmed by user

- AND plane = Fixed
- OR plane = Programmable



$$O_0 = I_0\ I_1\ \overline{I_2}\ I_3 + \overline{I_0}\ \overline{I_1}\ \overline{I_2}\ \overline{I_3} + I_0\ I_1\ \overline{I_2}$$

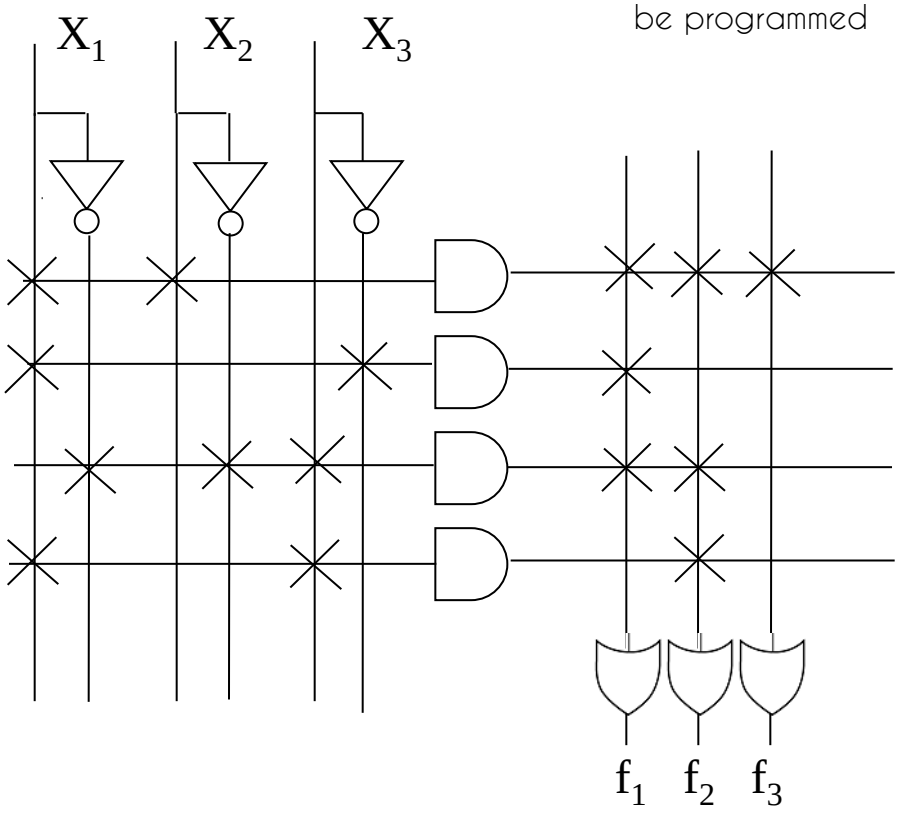
$$O_1 = \overline{I_0}\ \overline{I_1}\ I_2\ I_3$$

$$O_3 = \overline{I_0}\ \overline{I_1}\ \overline{I_2}\ \overline{I_3} + I_0\ I_1\ \overline{I_2}$$

6.3 Programmable Logic Devices

PLA ARCHITECTURE

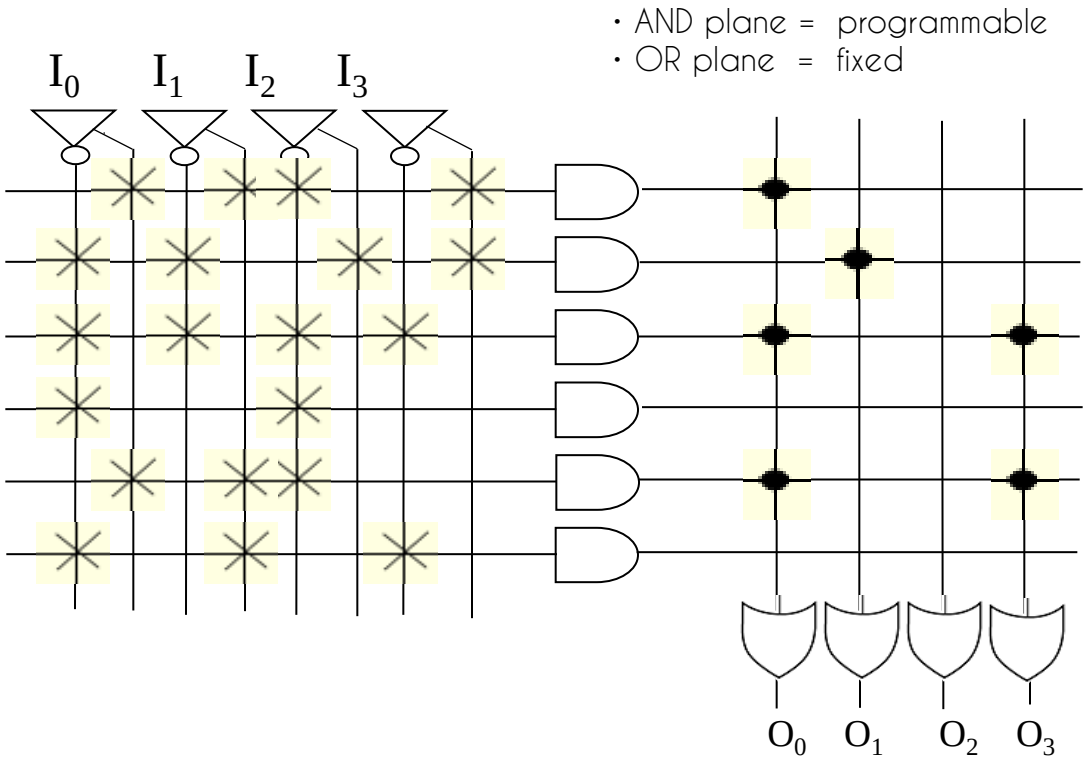
- Both AND & OR plane can be programmed



$$f_1 = X_1 X_2 + X_1 \overline{X_3} + \overline{X_1}\,\overline{X_2} X_3$$

6.3 Programmable Logic Devices

PAL ARCHITECTURE



$$O_0 = I_0\ I_1\ \overline{I_2}\ I_3 + \overline{I_0}\ \overline{I_1}\ \overline{I_2}\ \overline{I_3} + I_0\ I_1\ \overline{I_2}$$

Summaries of differences between Programmable ROM (PROM), *Programmable Array Logic* (PAL), and *Programmable Array Logic* (PLA)

PROM	PAL	PLA
AND array (hardwired)	AND array (programmable)	AND array (programmable)
OR array (programmable)	OR array (hardwired)	OR array (programmable)

EXERCISES

Programmable Logic Devices

1. List TWO (2) types of ASIC's design methodology.
2. Interpret about Gate-Array, standard cell and Programmable Logic Devices (PLD).
3. Draw the tree diagram of integrated circuit design methodologies.
4. Define gate and circuit level in the level of abstraction design.
5. Sketchthe floor plan of the gate array and standard cell.
6. Demonstrate the differences in a table of the design methodology between a Full Custom and a PLD based on its design cost, chip size, operation speed and power dissipation.
7. Illustrate a Programmable Array Logic (PAL) using the following functions:

$$f_1 = \overline{x_1}\ \overline{x_2}x_3 + x_1\overline{x_2}\ \overline{x_3}$$

$$f_2 = \overline{x_1}\ \overline{x_3} + x_1\ \overline{x_3}$$

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