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Thermal design optimization of electronic circuit board layout with transient heating chips by using Bayesian optimization and thermal network model

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ABSTRACT

This paper describes a method combining Bayesian optimization (BO) and a lumped-capacitance thermal network model that is effective for speeding up the thermal design optimization of an electronic circuit board layout with transient heating chips. As electronic devices have become smaller and more complex, the importance of thermal design optimization to ensure heat dissipation performance has increased. However, such a thermal design optimization is difficult because various trade-offs associated with packaging and transient temperature changes of heat-generating components must be considered. This study aims to improve the performance of thermal design optimization by artificial intelligence. BO using a Gaussian process was combined with the lumped-capacitance thermal network model, and its performance was verified. As a result, BO successfully found the ideal circuit board layout as well as particle swarm optimization (PSO) and genetic algorithm (GA) could. The CPU time for BO was 1/5 and 1/4 of that for PSO and GA. In addition, BO found a non-intuitive optimal solution in approximately 7 min from 10 million layout patterns. It was estimated that this was 1/1000 of the CPU time required for analyzing all layout patterns.

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1. Introduction

In recent years, electronic devices and energy storage systems have become smaller (thinner), and their internal structures have become more complex; therefore, ensuring their good heat dissipation performance has become an issue. Thermal design and temperature control are becoming key elements in improving product performance and reliability [1,2]. For example, temperature suppression methods combining composites, fins, fluids, and phase change materials (PCMs) among others have been studied [3–11]. Most of the heat generated inside a small electronic device is dissipated through the printed circuit board (PCB) on which the heat-generating components are mounted and then dissipated to its surroundings. To improve this heat dissipation, i.e., the cooling performance, the layout of the heat-generating components mounted on the PCB (hereinafter referred to as the PCB layout) must be optimized. This optimization process requires consideration of trade-offs due to various constraints in product packaging and a large number of layout patterns, making the search for an optimal solution difficult. Therefore, the development of efficient thermal design methods using artificial intelligence (AI) has been reported [12–19]. Wang et al. [12] used ant colony optimization (ACO) to optimize the PCB layout. Alexandridis et al. [13] applied particle swarm optimization (PSO) to a similar PCB layout optimization. Ismail et al. [14] used a genetic algorithm (GA) for a similar PCB layout optimization. The reported studies show the feasibility of metaheuristic algorithms for PCB layout optimization although these algorithms have issues such as convergence to a local solution and difficulty to determine appropriate hyperparameters, depending on the optimization problems [20–23].

Bayesian optimization (BO) using Gaussian processes has recently been applied for optimal design of various devices and systems [24–31]. It has been reported that BO does not easily fall into a local solution [32,33], and its algorithm is provided as a programming library for ease of use. Therefore, BO may be effective for the PCB layout optimization problem; however, its effectiveness has not been verified so far, to the best of the authors' knowledge.

In this study, BO is combined with a lumped-capacitance thermal network model and applied to PCB layout optimization prob-

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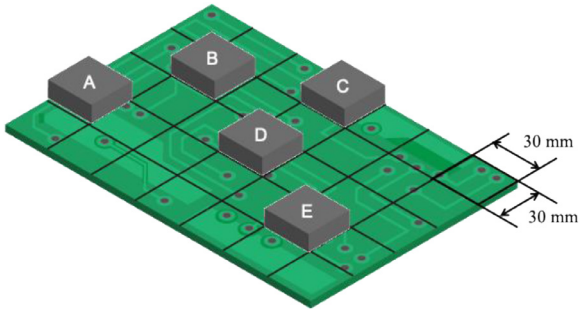


Fig. 1. Printed circuit board (PCB) model consisting of board and five heating chips (A-E) (the electronic circuit pattern illustration on the board is just a texture and not considered in the simulation).

Table 1
Specification of circuit board model components.

	Dimensions [mm]	Max. heating power [W]	Integrated heating energy [Wh]
Board	210 × 150 × 1	N/A	N/A
Chip A	30 × 30 × 10	4.1	1.54
Chip B	30 × 30 × 10	4.0	1.25
Chip C	30 × 30 × 10	3.8	1.03
Chip D	30 × 30 × 10	3.0	0.83
Chip E	30 × 30 × 10	2.0	0.50

lems, and its effectiveness is verified by comparing it with other algorithms (PSO and GA). Furthermore, the optimization was carried out based on unsteady state temperature simulations in which time variations of heating power and temperature of the components were taken into account. In the reported studies on PCB layout optimization, the heating power of the heating components is assumed to be constant, and the layout optimization is performed using the temperature under steady-state conditions. However, in actual PCBs especially for power units in electric vehicles, the heating power often varies with time. Therefore, the present study unveils the performance potential of BO in more complicated optimization cases than those in reported studies.

2. Simulation model and problem setting

2.1. Thermal network model for PCB layout optimization

A lumped-capacitance thermal network model (TNM) was used for the transient temperature simulation of a PCB. It is a model based on the analogy between electrical circuits and heat transfer phenomena and is widely used in design simulation of thermal systems because it allows unsteady heat transfer simulation of systems without using fine computational mesh and time-consuming complex fluid simulations [34–40].

Fig. 1 shows the PCB model to be optimized. There are five heat-generating components (hereafter referred to as heating chips or chips). The dimensions, maximum heating power, and integrated heating energy (for $0 \leq t \leq 1800$s) of the PCB and each chip are summarized in Table 1. Fig. 2(a) shows the TNM of the PCB, which consists of 5 × 7 computational nodes. Fig. 2(b) shows the TNM of the heating chip. It consists of a central semiconductor chip core (red-colored 1 node), the heat source, and its surrounding resin chip package (6 nodes). The thermophysical properties of the model components are summarized in Table 2. As shown in Fig. 3, it was assumed that the heating power of each chip varied with time. Each chip has different time-varying characteristics, total heating power, which is the sum of the heating power of each chip (black line), and peaks at $t = 1047$s. This particular power dissipation pattern was randomly determined so that the sum of the heating power has a peak during the simulation period. Such a pattern can be a possible case for PCBs with semiconductor chips in power units of electric vehicles.

Table 2
Thermophysical properties of circuit board model components.

	Board	Chip package	Chip core
Materials	Aluminum	Epoxy resin	Silicon
Specific heat [J/g·K]	0.9	1.5	0.77
Density [g/cm^3]	2.7	1.2	2.3
Conductivity [W/m·K]	170	0.3	156

Table 3
Simulation conditions.

Initial temperature of all components	25 °C
Air temperature	25 °C (Constant)
Boundary conditions	Board-Air: Natural convection Chip-Air: Natural convection Board side and bottom: Adiabatic
Heat transfer coefficient for natural convection	10 W/m^2·K

Because the lumped-capacitance model is used, the heat capacitance is connected to every node in Fig. 2(a) and (b), although their circuit diagram symbols are omitted in the figures. It is noted that the circuit symbols of thermal resistance between the nodes and the ambient air are also omitted. In TNM, the temperature at the nth node is calculated as:

$$\sum_{i=1}^{l} Q_i = \frac{dT_n}{dt} m_n c_n \tag{1}$$

where Q_i [W] is the amount of heat flowing from the neighboring nodes, l is the number of neighboring nodes, T_n [K] is temperature, t [s] is time, m_n [kg] is mass, c_n [J/kg•K] is the specific heat, and the subscript indicates the number of nodes. Q_i is calculated by the following equation:

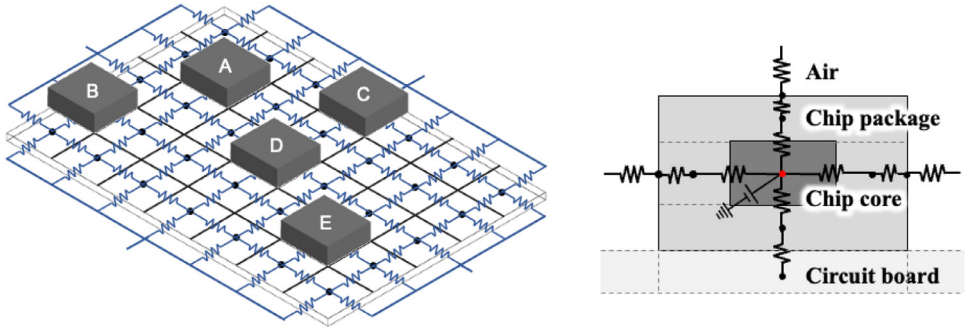
$$Q_i = \frac{\Delta T_i}{R_i} \tag{2}$$

ΔT_i [K] is the temperature difference between the nth node and the adjacent node, R_i [W/K] is the thermal resistance considering conduction and convection, which are calculated by the following equations [36].

$$R_{conv} = \frac{1}{hA} \tag{3}$$

$$R_{cond} = \frac{d}{\lambda A} \tag{4}$$

where R_{conv} [K/W] is the thermal resistance of convection, R_{cond} [K/W] is the thermal resistance of conduction, h [W/m^2·K] is the heat transfer coefficient, λ [W/m·K] is the thermal conductivity, A [m^2] is the heat transfer area, and d [m] is the distance between nodes. The thermal resistance due to thermal radiation is neglected here. The initial and boundary conditions are listed in Table 3. Natural convection with $h = 10$ W/m^2·K was assumed at all board-air and chip-air boundaries. The bottom and side of the board were assumed to be adiabatic. In this study, the contribution of radiation heat transfer was neglected to simplify the simulation model. Some PCB thermal design literature also ignores the radiation heat transfer. However, in the case of chip cooling by natural convection, if the temperature difference between the chip and the surface of the surrounding object (e.g., the inside wall of the case) is large, the radiation heat flux can be comparable to or larger than the convective heat flux. In such a case, the radiation heat transfer should not be ignored.



(a) PCB component with heating chips (b) Chip component

Fig. 2. Lumped-capacitance thermal network model for PCB model. The nodes for ambient air, thermal resistances between the board and chip surface to the air, and heat capacity of board and chip nodes are omitted in Fig. 2(a). Heat capacity of each node are omitted in Fig. 2(b)

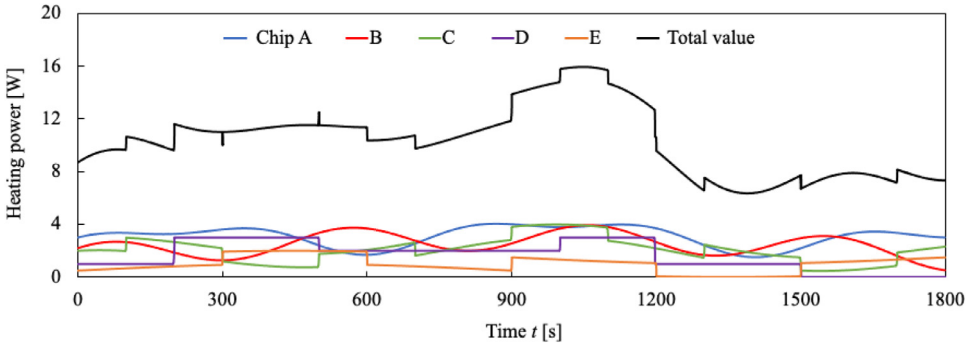


Fig. 3. Time-variations of heating power of five heating chips (A-E) in circuit board model.

This model was implemented in MATLAB/Simulink, and an unsteady heat transfer simulation was performed to obtain the temperature change characteristics of each node. The chip temperature is defined as the average temperature over the nodes within the chip component. Fig. 4 shows the TNM in MATLAB/Simulink. Fig. 4(a) shows the TNM of PCB with heating chips, in which the chip components are connected to the network at their positions on the PCB. Fig. 4(b) shows the TNM of the chip components. The placement of the heating chip can be easily enabled or disabled by changing the setting values of thermal resistance components and heat capacity components enclosed by the dotted black line to zero. This method makes it possible to change the PCB layout with less computational effort. Moreover, MATLAB provides a fast solver for multiple simultaneous linear equations given by Eq. (1), contributing to fast computation of the unsteady heat transfer phenomenon.

2.2. Optimization problem setting

The target of the optimization is the PCB layout, that is, the placement pattern of five transient heating chips A to E. In actual product design, there may be restrictions on chip placement depending on the functions of the devices. To simulate this situation, two restrictions on chip placement are given as (i) placeable area for each chip and (ii) distance between chips. In restriction (i), each chip can only be placed in a mesh defined by a frame of the same color as the color of the chip symbol, as shown in Fig. 5. In other words, each chip can only be placed within a specified area. In restriction (ii), the distance between the nodes at the center of the chips must be less than or equal to the values shown in Table 4. For example, in Fig. 4, the distance between chips A and B is 51.96 mm, which satisfies the restricted value (90 mm).

Table 4
Restriction (ii).

Max. distance between the chips [mm]	
Chips A-B	90
Chips B-C	90
Chips A-D or D-E	90

Optimization was performed so that the value of the following objective function $f(x)$ was minimized:

$$f(x) = w\ \max\{T_{\text{mean}}(t)\} + (1-w)\ \max\left\{T_{\text{high}}(t)\right\} \quad (5)$$

where x indicates one of the PCB layouts. $T_{\text{mean}}(t)$ is the mean chip temperature, that is, the average chip temperature over the five chips at time t; $T_{\text{high}}(t)$ is the highest chip temperature among the five chips at time t; max{} is the maximum value during the simulation time period ($0 \le t \le 1800$s); w is the weight coefficient; with the optimization being performed for three cases namely: $w = 1$, 0, and 0.5. This methodology is called the weighted sum method and commonly used for multi-objective optimization [41,42]. The objective function for $w = 1$, 0, and 0.5 is $f(x) = \max\{T_{\text{mean}}(t)\}$, $f(x) = \max\{T_{\text{high}}(t)\}$, and $f(x) = [\max\{T_{\text{mean}}(t)\} + \max\{T_{\text{high}}(t)\}]/2$, respectively.

3. Validation of the simulation model

Prior to performing the optimization and to confirm the validity of the present lumped-capacitance TNM, three-dimensional (3D) finite element method (FEM) simulations under the same model and conditions were conducted, and the results were compared with the results obtained by TNM. The commercial software ANSYS was used for the FEM simulation. FEM simulation is a widely used simulation in the field of heat transfer engineering. The FEM simulation generally provides reliable results; however, it requires a

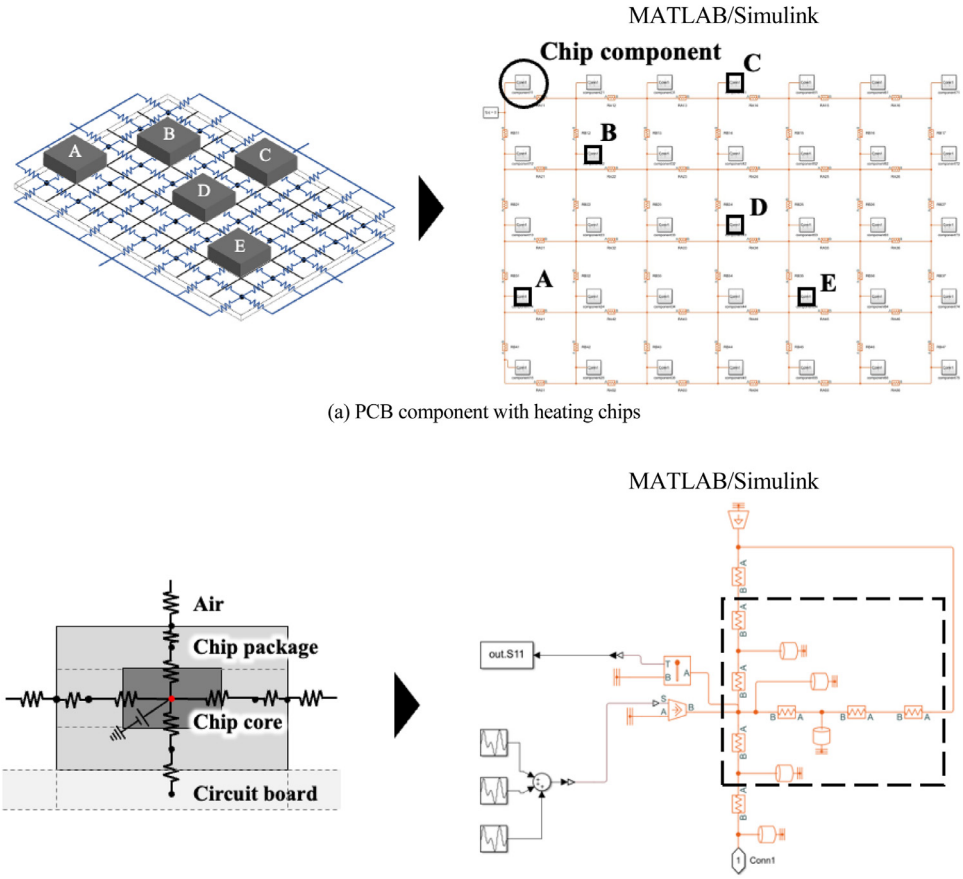


Fig. 4. Thermal network model implementation in MATLAB/Simulink. The right figure shows the MATLAB/Simulink model of the left figure..

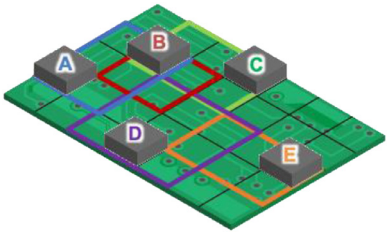


Fig. 5. Restriction (i): Colored mesh depicts placeable areas for each chip with the same colored symbols.

fine 3D computational mesh and a fine time step, resulting in high computational cost. The number of computational meshes used in the FEM model was set to 3630. By contrast, the number of computational nodes in TNM is 95. A comparison of the results from FEM and TNM is shown in Figs. 6 and 7. The upper and bottom figures in Fig. 5(a)–(d) show the FEM and TNM results of temperature distribution at elapsed times t = 250 s, 750 s, 1250 s, and 1800 s, respectively. The TNM results depict the mean temperature over the surface nodes within each mesh. The trends of the temperature distributions in both simulations agreed well. For a more quantitative comparison, Fig. 7 shows a comparison of the time variation of chip temperature, that is, the average temperature of the chip component, in both simulations. For FEM, it is the volume average temperature of computational meshes in the chip core, and for TNM, it is the temperature of the red dot of the lumped capacitance chip core shown in Fig. 2(b). The trends of each chip were consistent. The root mean square error (RMSE) between the chip temperature profile obtained by the TNM and FEM for each chip ranges between 0.45—1.12 °C. These results show that the present TNM has sufficient validity for the PCB layout optimization, although the spatial resolution of temperature distribution is lower than that of FEM simulations. Moreover, the CPU time of the TNM was approximately 10 times faster than that of the FEM, although FEM simulation was conducted using Xeon E5–2620v3 × 2 (RAM:64 GB), and TNM simulation using AMD Ryzen9 3950 × 3.49 GHz (RAM:16 GB).

4. Applying Bayesian optimization

The thermal design optimization problem can be formulated as an optimization of the black box continuous functions $f(x)$ as follows:

$$x = \mathrm{argmin}_x f(x) \tag{6}$$

where x is the input variable, and $f(x)$ denotes the objective function of Eq. (5). The de-facto standard model for black-box optimization is BO with a Gaussian process. Bayesian optimization (BO) is a popular framework for optimizing the black box function owing to its sample efficiency. The Gaussian process has been widely applied to solve real-world problems such as the prediction of thermal systems due to its ability to capture non-linearity and quantify uncertainty [43–45]. Due to such characteristics, a Gaussian process is often selected to model the unknown objective function of BO. In BO, $f(x)$ is a stochastic process, which is assumed to follow a Gaussian process, that is, the following Eq. (7), where $\mu(x)$ is the mean function (of the objective function at point x), $\sigma(x)$ is the covariance function (of the objective function at a point x), and

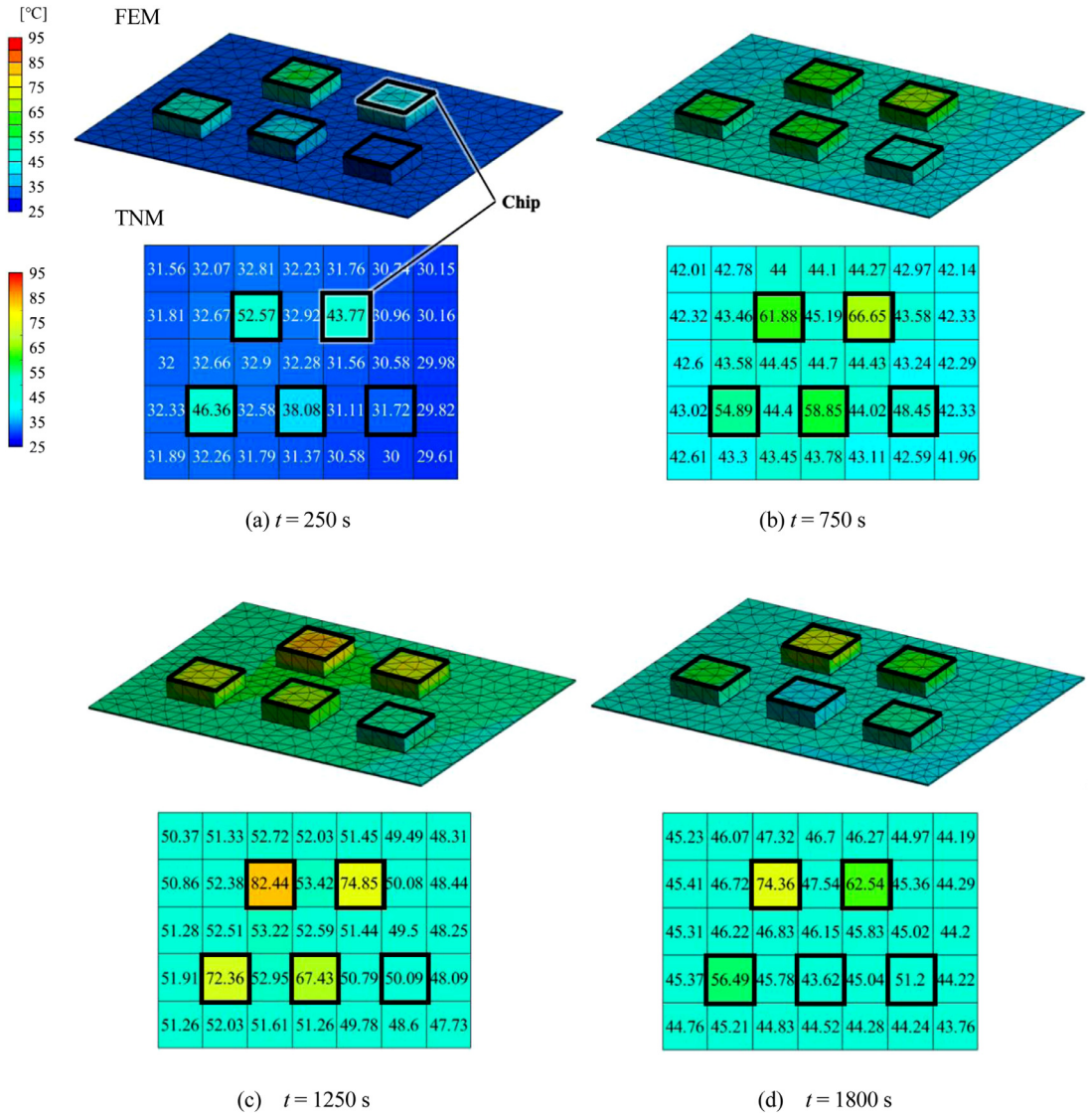


Fig. 6. Comparison of simulated temperature distributions between FEM (upper figure) and TNM (bottom figure) at t = 200 s, 500 s, 1000s, and 2000s.

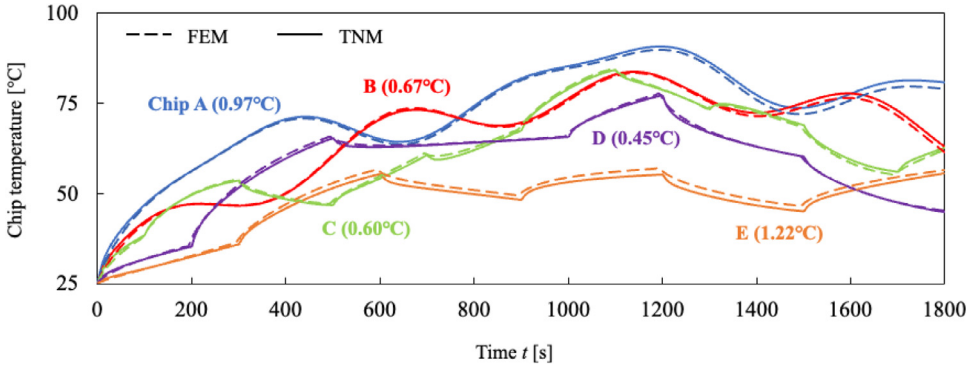
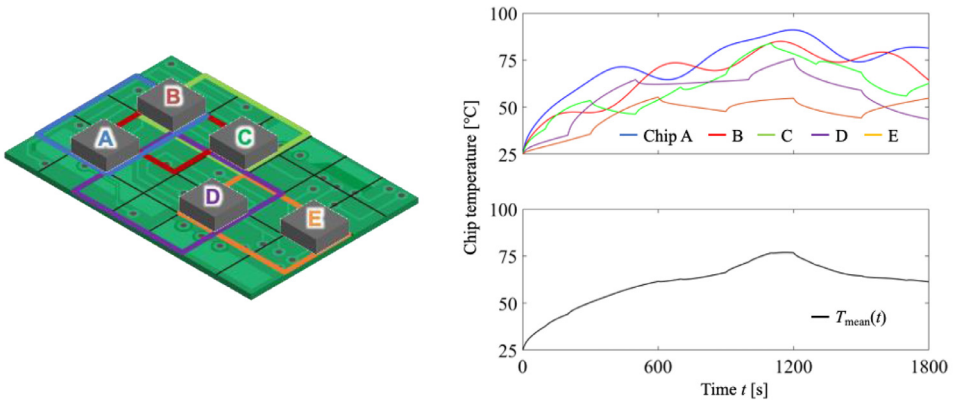


Fig. 7. Comparison of simulated chip temperature between FEM and TNM. RMSE between FEM and TNM for each heating chip is shown in parentheses.

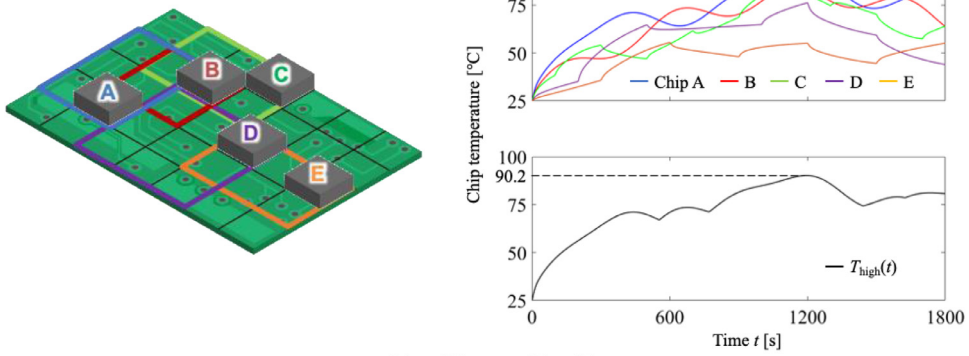
$k(x, x')$ is the kernel function.

$$f(x) \sim GP(\mu(x), \sigma(x)) = GP\left(\mu(x), k\left(x, x^{'}\right)\right) \tag{7}$$

In this method, the posterior distribution of $f(x)$ is calculated from the currently observed data based on Eq. (7), and the next search point is determined using the acquisition function based on the information of the peripheralized predicted distribution. This process is repeated to find the optimal solution [46–48].The Matérn5/2 kernel [33] was used as well as an expected improvement (EI) [32,33]. The combination of EI and the Matérn5/2 kernel is often used in practical applications [29]. In simulation, the "bayesopt" function of MATLAB library was used. Optimization with PSO and GA was also performed and compared with BO. The "particle swarm" and "ga" functions of the MATLAB library were



(a) $f(x) = \max\{T_{mean}(t)\}$



(b) $f(x) = \max\{T_{high}(t)\}$

Fig. 8. Comparison of optimized component layouts by BO for different objective functions.

Table 5
Hyperparameters of GA and PSO.

GA		
	Population size	50
	Selection	Stochunif
	Mutation rate	0.01
	Crossover rate	0.8
PSO		
	Swarm size	50
	Cognitive parameter	1.49
	Social parameter	1.49

Table 6
Comparison of optimization results (temperature).

Objective function (Optimization to minimize $f(x)$)	$f(x)$ of the optimized PCB layout [C]			
	Searching all layout patterns	BO	PSO	GA
	76.88	←	←	←
$f(x) = \max\{T_{mean}(t)\}$				
$f(x) = \max\{T_{high}(t)\}$	90.20	←	←	←
	83.68	←	←	←
$f(x) = [\max\{T_{mean}(t)\} + \max\{T_{high}(t)\}]/2$				

Table 7
Comparison of optimization results (CPU time).

Objective function (Optimization to minimize $f(x)$)	CPU time to obtain optimized PCB layout [s]			
	Searching all layout patterns	BO	PSO	GA
	9836	183	866	691
$f(x) = \max\{T_{mean}(t)\}$				
$f(x) = \max\{T_{high}(t)\}$	↑	163	738	438
	↑	62	328	495
$f(x) = [\max\{T_{mean}(t)\} + \max\{T_{high}(t)\}]/2$				

used for PSO and GA, respectively. The hyperparameters of PSO and GA are shown in Table 5, which were the typical hyperparameter settings used here [49–51]. The total number of iterations was set to 200 for all algorithms. To determine the true optimal PCB layout (henceforth, ideal layout), all 7776 layout patterns were searched and $f(x)$ for them were evaluated in advance. The performance of each algorithm was verified by comparing their optimized layout with the ideal layout. The CPU time consumed by each algorithm was compared. All the simulations were conducted on a Windows workstation with AMD Ryzen9 3950 × 3.49 GHz and 16 GB memory. Note that previous studies [12–18] did not make comparisons with the ideal layout.

5. Optimization results

Tables 6 and 7 show the comparison of optimization results, that is, values of $f(x)$ of the optimized PCB layout, and CPU time, for each algorithm including all layout pattern searches. With 200 iterations, three algorithms reached the same layout as the ideal layout regardless of the $f(x)$ case. BO reached the ideal layout in approximately 1/150–1/90 of CPU time for all layout pattern searches, and in approximately 1/5 and 1/4 of the CPU time of PSO and GA, respectively. The swarm size and the population size affect the CPU time of PSO and GA, respectively. In this case, because

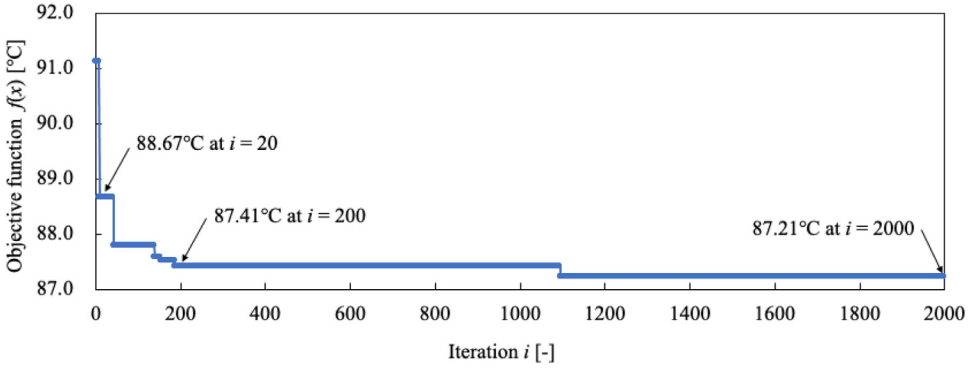


Fig. 9. Optimization progress by BO.

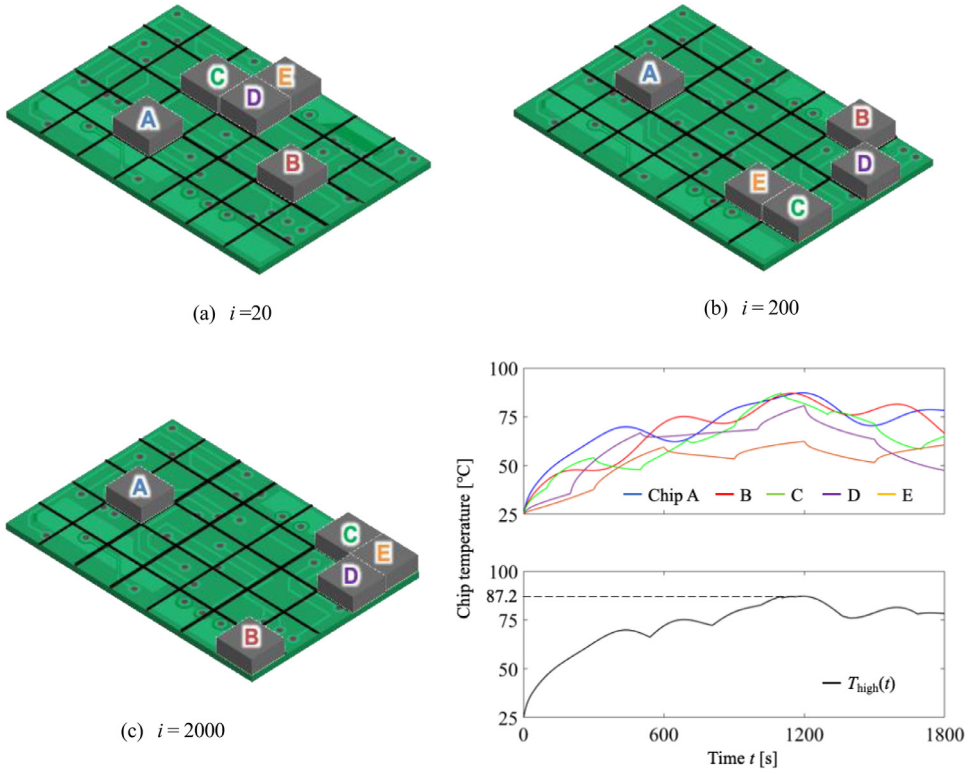


Fig. 10. Optimized component placement by BO w/o restrictions (i) and (ii).

both sizes are set to 50, PSO and GA must evaluate 50 layout patterns per iteration. By contrast, BO evaluated one layout pattern per iteration. As the transient temperature simulation per layout pattern takes a long CPU time, PSO and GA must take a longer CPU time per iteration than BO. This is the major reason for the increase in CPU time for PSO and GA. By the authors' trial, reduced population and swarm size (i.e., population size and swarm size of 5) actually shortened the CPU time but resulted in incorrect optimization. The performance of PSO and GA may be improved by further careful tuning of hyperparameters; however, this is time consuming. It is noted that BO was still faster than PSO and GA with population and swam size of 5. These results imply that BO can be a time-efficient algorithm for PCB layout optimization coupled with the transient temperature simulation.

Fig. 8(a) and (b) show the optimized layouts (which are identical to the ideal layouts) obtained by BO in three $f\ (x)$ cases, respectively. In the figures, the corresponding time variations of each chip temperature and $T_{mean}(t)$ or $T_{high}(t)$ are also shown. In Fig. 8(a), $T_{mean}(t)$ reaches the maximum value at approximately t = 1200s. This maximum value is the temperature of Chip A, which has the highest total heat generation, as shown in Table 1. In this case, because the chips should be evenly distancing to minimize $f\ (x) = \max\{T_{mean}\ (t)\}$, it would be easy for us to predict a similar layout pattern intuitively. By contrast, in Fig. 8(b), with the optimization to minimize $f\ (x) = \max\{T_{high}\ (t)\}$, Chips B and C are arranged close to each other, and Chip A is mostly distancing from the other chips, which would not be easy for us to predict intuitively. This indicates that the optimized layouts are reasonable and that the thermal design optimization using BO is effective.

6. Applying BO to extended problem settings

In the actual thermal design of PCBs, the number of layout patterns can be even greater. To test the performance of BO in such a case, BO was applied to an extended problem setting in which the restrictions (i) and (ii) described in Section 2.2 are removed. In this case, the number of possible layout patterns is approximately 10 million. The optimization for $f\ (x) = \max\{T_{high}\ (t)\}$ case

was performed. Fig. 9 shows the evolution of the value of the objective function with respect to the number of iterations. The values of $f(x)$ at the 20, 200, and 2000 iterations are shown in the graph. Fig. 10 shows the corresponding optimized layouts and the time variations of the chip temperature and $T_{high}(t)$ for the optimized layout at 2000 iterations. From Fig. 9, the value of $f(x)$ is updated as the number of iterations increases, reaching 90% of the 2000 iterations' value at 200 iterations. T_{high} at 200 and 2000 iterations were reduced by 2.79 °C and 2.9 °C, respectively, compared to the T_{high} (90.20 °C) under restrictions (i) and (ii), as shown in Table 6 in Chapter 4. Fig. 10 shows that Chips A and B were optimized to maintain distance from the other chips. This is because the heating power of Chips A and B is relatively larger, as shown in Table 1, so they are placed farther distancing from each other to lower T_{high}. Comparing the temperature trends in Figs. 10(c) and 8(b), the temperature of Chip A decreases. The CPU times for 200 and 2000 iterations were 434 s and 16676 s, respectively. Based on the results in Chapter 5, the estimated CPU times for 2000 iterations for PSO and GA are 160,000 s, which is approximately 10 times longer than that of BO. Similarly, the CPU time required for the simulation of all layout patterns search was estimated to be about 140 days, and BO was able to optimize at approximately 1/1000 of the time for all layout pattern searches. From these results, the high speed of BO was confirmed in the extended problem setting. However, it is reported that the computational complexity of BO tends to increase with the number of iterations [48]. This fact was also confirmed by the present result. The CPU time for 2000 iterations was 38 times higher than that for 200 iterations. This characteristic should be considered when performing the optimization by BO. In the present case, 200 iterations were found to be appropriate to obtain a nearly optimal layout pattern.

7. Conclusion

Bayesian optimization (BO) combined with the lumped-capacitance TNM was applied to the layout optimization of an electronic PCB with transient heating chips, and its effectiveness was verified by fundamental case studies. To evaluate the value of the objective function of the examined layout, a transient heat transfer simulation was performed per layout taking into account the different temporal variations of the heating power of the heat-generating chips. As a result, BO reached the ideal layout in approximately 1/150–1/90 of CPU time for all layout pattern searches and in approximately 1/5 and 1/4 of the CPU time of other algorithms (PSO and GA), respectively. Furthermore, BO was applied to the extended problem setting with possible layout patterns of 10 million. BO found a reasonably best layout, which achieved 90% of the objective function value of 2000 iterations, at 200 iterations in approximately 7 min only. All layout pattern searches would have required 140 days, and BO took only 1/1000 of that time for optimization. In addition, by comparing it with other algorithms (PSO and GA), the effectiveness of the present method was demonstrated for the PCB layout optimization problem that requires a transient heat transfer simulation. In future research, it will be necessary to upgrade to a more realistic model that also considers more complicated circuit board structures such as multi-layered structures (chip, die bonding, heat spreader, etc.) and contact thermal resistances between the layers and also conditions such as temperature dependent heat transfer coefficient.

Declaration of Competing Interest

The authors declare that they have no conflict of interest.

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Availability of data and material

All data and material is available upon request.

Code availability

Codes are available upon request.

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