

A comprehensive circuit and modulation design of mixed frequency conversion cascaded power electronic transformer

Yonghai Xu^a, Xueyin Zhang^b, Xu Dong^c, Abubakar Siddique^{d,*}, Waseem Aslam^e

^a State Key Laboratory of Alternate Electrical Power System with Renewable Energy Sources (North China Electric Power University), Changping District, Beijing 102206, China

^b Sichuan Energy Internet Research Institute, Tsinghua University, Chengdu 610213, China

^c Jinan Power Supply Company, Shizhong District, Jinan 250013, China

^d Department of Electrical and Biomedical Engineering, Khwaja Fareed University of Engineering & Information Technology (KFUEIT), Rahim Yar Khan 64200, Pakistan

^e Department of Electrical, Electronics and Computer Systems, University of Sargodha (UOS), Sargodha 40100, Pakistan

ARTICLE INFO

Keywords:

Power electronic transformer (PET)
Mixed frequency conversion
Circuit design
Modulation method

ABSTRACT

The power electronic transformer (PET) is one of the promising equipment of the energy Internet. In a distributed network, cascaded (cascaded full-bridge, CFB)-type PETs can withstand high-voltage stress and contain a low-voltage DC (LVDC) port, which provides access for distributed generation (DG). However, the hardware cost of the traditional CFB-type topologies remains high, and structure compactness can still be improved. The recently presented mixed-frequency conversion cascade PET (MFCC-PET) is one of the promising solutions. In this study, a comprehensive circuit design of MFCC-PET, a low-voltage distortion nearest-level pulse width modulation (NL-PWM), and a sub-module (SM) voltage balancing strategy for the proposed modulation method under mixed-frequency conversion are presented. A 100 V/2,000 W MFCC-PET prototype is built based on the above analysis and successfully placed into operation.

1. Introduction

THE PET is an essential equipment with the abilities of power conversion, electrical isolation, voltage transformation, power factor correction, and power flow control. Moreover, it contains an LVDC port, which provides access for DG.

PETs are classified into three [1], namely, single-stage [2,3], two-stage [4–6], and three-stage structures [7–16]. The three-stage structure contains DC stage at HV and LV sides, providing strong controllability, good power quality characteristics, and multiple ports. Thus, it is widely studied.

In medium-/high-voltage applications, a substantial device number of high-frequency transformers (HFTs) and power switches in three-stage topologies result in two problems: 1) High hardware cost. HFTs and power switches dominate the cost of PET hardware [17], and reducing the device number of HFTs and power switches contributes to reduced cost [1]; 2) Not compact enough structure. In medium- and high-voltage applications, although the volume of a single HFT is small, too many HFTs occupy a large volume because of insulation gaps between each device [17]; thus, reducing the device number of HFTs can

increase the power density of PET. Power switches with different current capacities can be accessorized in the same package [18,19]. Using one power switch with a high current capacity rather than using several power switches with a small current capacity can improve the compactness of the converter valve.

Cost and volume have become the main factors affecting the application of PET [1]. Reducing costs and improving structural compactness have become essential requirements for PET in real applications.

A two-stage CFB topology is proposed by [20], in which DC capacitors exist on the HV and LV sides of HFT; this topology reduces the number of HFTs and LV-side power switches. The main advantages and benefits of this topology are lower hardware cost and compact structure due to the small device number of HFTs and power switches. Moreover, it has fewer high-frequency conversion stages, making the consistency of the parameters easy to achieve. The HV side of this topology achieves a single-stage low-frequency AC to high-frequency AC power conversion by generating line-frequency and high-frequency voltages through CFB at the same time; thus, it is named MFCC-PET in this work. Similar studies can be found in [21].

The above research on MFCC-PET has already made some progress in

* Corresponding author.

E-mail address: dr.abubakar@kfueit.edu.pk (A. Siddique).

<https://doi.org/10.1016/j.ijepes.2024.109784>

Received 7 May 2023; Received in revised form 12 October 2023; Accepted 3 January 2024

Available online 13 January 2024

0142-0615/© 2024 The Authors. Published by Elsevier Ltd. This is an open access article under the CC BY license (<http://creativecommons.org/licenses/by/4.0/>).

the aspects of topology, function principle, and performance comparison. In this work, the studies of MFCC-PET in the following aspects are discussed: (1) A circuit design is presented. (2) A low-voltage distortion NL-PWM method is proposed, and the implementation of mixed frequency conversion is presented on this basis. (3) Experiments are carried out based on a 100 V/2,000 W prototype.

2. Circuit design

2.1. Topology

The topology of MFCC-PET is shown in Fig. 1 [20]. The three-phase configuration is a combination of three single-phase ones.

Fig. 1a shows a simple single-phase structure of the MFCC-PET. The CFB functions as a multi-frequency voltage source. Filter inductor L_f serves as a low path filter (LPF). Resonant capacitor C_r and inductor L_r operate as a band pass filter (BPF), wherein L_r can be integrated into HFT Tr.

The MFCC-PET is based on the principle of mixed-frequency conversion: Part of the SMs output a line frequency sinusoidal voltage, and the other part of the SMs output same-phase square-wave voltage. A filter circuit separates the low-frequency components and high-frequency components output by CFB. Therefore, the energy exchange with the power grid and HFT can be realized at the same time. In this way, the series connection of two-stage sub-modules can be avoided, thereby reducing the number of HFT and power-switching devices.

The three single-phase bridge arms in Fig. 1a are star-connected, as shown in Fig. 1b. Three separated HF paths on the primary side are used in the type 1 circuit. The DC ports of the three secondary-side full-bridge SMs (FBSMs) are parallel connected to provide a LVDC bus. The DC/AC in the LVDC bus, not shown in Fig. 1b, converts LVDC to LVAC.

Three single-phase PETs are combined to form a three-phase topology type 1 structure, as shown in Fig. 1(b). In the figure, the three phases of the LVDC side are connected in parallel to improve the flow capacity; the three phases can also be connected in series to improve the withstand voltage level. In terms of control, the high-frequency electricity output by the three-phase CFB on the high-voltage side is set to be in phase, and there is no neutral line without a zero-sequence path on the high-voltage side and high-frequency current will not be generated on the grid side.

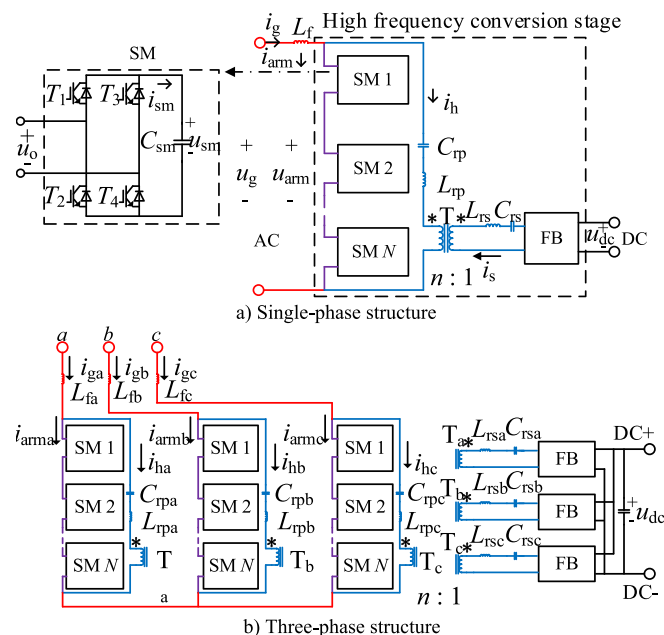


Fig. 1. Topology of MFCC-PET.

In order to further reduce the number of HFTs and the number of low-voltage side power switching devices, the three-phase resonant LC ends are connected to one point to form a midpoint, and the neutral line is drawn from the midpoint. The common point of the three-phase topology constitutes a type 2 structure as shown in Fig. 2. In this fig., L_{rx} ($x = abc$) and C_{rx} form a band-pass filter in series to limit the transmission of power frequency current and high-frequency associated current between phases; L_{rx} , C_{rx} , L_{rnp} , C_{rnp} , and low-voltage side neutral line inductance L_{rns} , Capacitor C_{rns} constitutes a band-pass filter to limit the injection of power frequency current and high-frequency associated current into the HFT.

Other benefits: (1) In the type 2 structure, the HFT is located in the neutral line, so there is no positive sequence and negative sequence current in the transformer current, which is beneficial to reduce the HFT current. (2) Type 2 structure has high-frequency interphase paths on the high-voltage side that can exchange three-phase energy on the high-voltage side without HFT, which is useful for three-phase unbalanced control and sub-module capacitor voltage fluctuation stabilization.

Considering the three-phase type 2 structure is a modification of the type 1 structure, in the following, the type 1 structure is studied.

2.2. Function principle

The following part describes the power decoupling of MFCC-PET to show how the input stage control of MFCC-PET can be same as CFB-PET.

For the CFB bridge arm, assuming that the number of SMs outputting square-wave voltage is δN (δ is the proportion of sub-modules outputting power frequency sine to the total, N is the total number of submodules. $0 < \delta < 1$, and δN is an integer), the number of SMs outputting the sinusoidal voltage is $(1-\delta)N$.

Thus, the sinusoidal voltage of bridge arm is:

$$u_{arm,g} = (1-\delta)MNU_{SM}\sin(\omega_g t + \varphi_g) \quad (1)$$

Where M is the modulation ratio, ω_g is the line frequency, φ_g is the initial angle, U_{sm} is the submodule voltage.

The RMS of the square wave voltage is:

$$U_{arm,h} = \delta NU_{SM} \quad (2)$$

For the input stage, according to the relationship between voltage, current and impedance (VCR), i_g can be obtained:

$$i_g = \frac{1}{L_f} \int (u_g - u_{arm,g}) dt = \frac{1}{L_f} \int [u_g - (1-\delta)MNU_{SM}\sin(\omega_g t + \varphi_g)] dt \quad (3)$$

Where u_g is the grid side phase voltage, L_f is the inductance value of the bridge arm; u_g is the grid side phase voltage, φ_g is the initial angle of

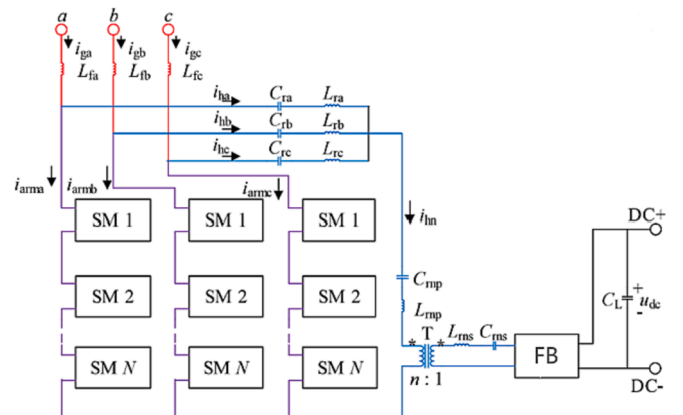


Fig. 2. Three-phase type 2 structure.

u_g .

According to (1) and (3), the instantaneous power between CFB and the network per phase is:

$$s_{CFB,g} = u_{arm,g} i_g =$$

$$\frac{u_{arm,g}}{L_f} \int [u_g - (1 - \delta)MNU_{SM} \sin(\omega_g t + \varphi_g)] dt \quad (4)$$

In which the magnitude of the active power is:

$$P_{CFB,g} = \frac{U_g U_{arm,g}}{\omega_g L_f} |\sin \theta| = \frac{(1 - \delta)MNU_{SM} U_g}{\sqrt{2} \omega_g L_f} |\sin \theta| \quad (5)$$

Where $U_{arm,g}$ is the bridge arm rms voltage, U_g is the grid side phase rms voltage, θ is the power angle.

The magnitude of the reactive power is:

$$Q_{CFB,g} \approx \frac{|U_{arm,g} - U_g| U_g}{\omega_g L_f} = \frac{|(1 - \delta)MNU_{SM}/\sqrt{2} - U_g| U_g}{\omega_g L_f} \quad (6)$$

From the above analysis, the power of the input stage only relates to the line-frequency sinusoidal voltage $U_{arm,g}$ without the high-frequency one. Therefore, the power decoupling character is achieved. Thus, the operating principle of the input stage of MFCC-PET is the same as that of CFB, as well as the control.

2.3. Circuit design

The following part describes the design method of the circuit components, including reactors and capacitors.

The HV-side CFB functions in unit power factor; thereby, the RMS of i_g is:

$$I_g = \frac{P_{CFB,g}}{U_g} \quad (7)$$

The high-frequency conversion stage contains an LC serial resonant tank, and the square-wave voltage on the HV and LV sides are in phase [20]. Under such open-loop control, HFT current i_{hx} ($x = a, b, c$) is in a quasi-sine wave, and the ZCS [27] of the LV-side power switches is obtained. The LVDC voltage can be adjusted within a small range by just changing the capacitor voltages of CFB.

Since the power balancing principle, ignoring the power loss, the power of the line-frequency port should be the same as the power of the high-frequency side:

$$I_h U_{arm,h} \frac{4}{\pi \sqrt{2}} = I_g U_g \quad (8)$$

Therefore:

$$I_h = \frac{I_g U_g \pi}{2 \sqrt{2} U_{arm,h}} \quad (9)$$

According to (7):

$$I_h = \frac{\pi P_{CFB,g}}{2 \sqrt{2} \delta N U_{SM}} \quad (10)$$

The RMS current of HFT depends on the LV-side loads, therefore, $P_{CFB,g} = P_L$, thus:

$$I_h = \frac{\pi P_L}{2 \sqrt{2} \delta N U_{SM}} \quad (11)$$

Where P_L is the absolute value of the power of LV-side loads per phase.

Furthermore, according to (7) and (11), as well as the power balance: $P_{CFB,g} = P_L$, the RMS of i_{arm} is:

$$I_{arm} = \sqrt{\left(\frac{P_L}{U_g}\right)^2 + \left(\frac{\pi P_L}{2 \sqrt{2} \delta N U_{SM}}\right)^2} \quad (12)$$

Ignoring the line-frequency voltage drop of the AC filter, $U_{arm,g} = U_g$, thereby $NU_{SM} = \sqrt{2} U_g / (M(1 - \delta))$, thereby, I_h can be rewritten as:

$$I_h = \frac{(1 - \delta) \pi M P_L}{4 U_g \delta} \quad (13)$$

Then, the RMS of i_{arm} is:

$$I_{arm} = \sqrt{\left(\frac{P_L}{U_g}\right)^2 + \left[\frac{(1 - \delta) \pi M P_L}{4 U_g \delta}\right]^2} \quad (14)$$

According to (1), N should satisfy:

$$N = \frac{\sqrt{2} U_{arm,g}}{(1 - \delta) M U_{SM}} \approx \frac{\sqrt{2} U_g}{(1 - \delta) M U_{SM}} \quad (15)$$

Assuming:

$$\begin{aligned} NI_{arm} &= \frac{\sqrt{2} U_g}{(1 - \delta) M U_{SM}} \sqrt{\left(\frac{P_L}{U_g}\right)^2 + \left(\frac{\pi P_L}{2 \sqrt{2} \delta N U_{SM}}\right)^2} = \\ &= \frac{\sqrt{2} U_g}{(1 - \delta) M U_{SM}} \sqrt{\left(\frac{P_L}{U_g}\right)^2 + \left[\frac{(1 - \delta) \pi M P_L}{4 \delta U_g}\right]^2} \\ &= \sqrt{\left[\frac{\sqrt{2} U_g P_L}{(1 - \delta) M U_{SM} U_g}\right]^2 + \left(\frac{\pi P_L}{2 \sqrt{2} \delta U_{SM}}\right)^2} = \\ &= \sqrt{\left[\frac{\sqrt{2} P_L}{(1 - \delta) M U_{SM}}\right]^2 + \left(\frac{\pi P_L}{2 \sqrt{2} \delta U_{SM}}\right)^2} = \frac{P_L}{U_{SM}} \sqrt{\frac{2}{(1 - \delta)^2 M^2} + \frac{\pi^2}{8 \delta^2}} \end{aligned} \quad (16)$$

Assuming:

$$\beta = \frac{2}{(1 - \delta)^2 M^2} + \frac{\pi^2}{8 \delta^2} \quad (17)$$

NI_{arm} decides the current capacity requirement for power switches. When P_L and U_{SM} are specified, the only factor that affects the value of NI_{arm} is β ; therefore, it can be used to investigate the influence of δ on the total current capacity of power switches. The universal used modulation ratios are investigated assuming $M = \{0.75, 0.80, 0.85, 0.90, 0.95\}$ [7–16]; according to (17), the curve of β versus δ can be obtained. Fig. 3 shows that when $\delta \in [0.4, 0.5]$, β is small. When $\delta = 0.5$, δN is an integer if N is even; it has good universality, such that $\delta = 0.5$ is studied in this work.

An equivalent circuit of the single-phase high-frequency conversion

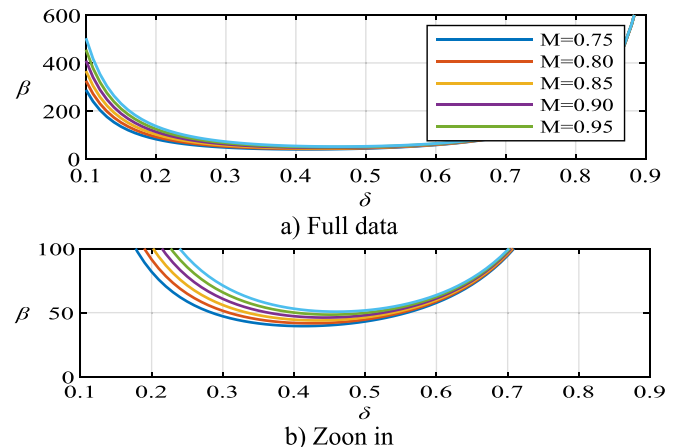


Fig. 3. Curve of β vs. δ .

stage is shown in Fig. 4. A full-bridge SM represents the CFB. R_r is the equivalent series resistance.

Design requirements for L_{rp} and C_{rp} are as follows: 1) Resonant angular frequency is ω_h ; 2) Reduce loss: the RMS of the line frequency current in the high-frequency conversion stage – I_{hg} is no larger than $\sigma_1 I_h$ ($\sigma_1 > 0$), 3) Reduce loss: the RMS of the switching harmonic currents in the high-frequency conversion stage – I_{hs} is no larger than $\sigma_2 I_h$ ($\sigma_2 > 0$), and 4) Reduce voltage stress: the peak of resonance voltage across L_{rp} and $C_{rp} - U_r$ is no larger than $\sigma_3 U_g$ ($\sigma_3 > 0$).

Normally, the power loss on R_r is small compared with that on the power switch. R_r can be ignored, and (18) can be obtained according to (1):

$$\frac{1}{\sqrt{L_{rp} C_{rp}}} = \omega_h \quad (18)$$

Similarly, (19) can be obtained according to (2):

$$\frac{U_g}{\omega_g C_{rp} - \omega_g L_{rp}} \leq \sigma_1 I_h \quad (19)$$

Combining (18) and (19), (20) can be obtained:

$$L_{rp} \geq \frac{U_g \omega_g}{\sigma_1 I_h (\omega_h^2 - \omega_g^2)} = \frac{4U_g^2 \omega_g}{\sigma_1 \pi M P_L (\omega_h^2 - \omega_g^2)} = L_{rp, \min} \quad (20)$$

Similarly, according to (4), (21) can be obtained:

$$U_r = \sqrt{2} I_h \omega_h L_{rp} = \frac{\sqrt{2} \pi M P_L \omega_h L_{rp}}{4 U_g} \leq \sigma_3 U_g$$

$$L_{rp} \leq \frac{2\sqrt{2} \sigma_3 U_g^2}{\pi M P_L \omega_h} = L_{rp, \max} \approx \frac{\omega_h \sqrt{2} \sigma_3}{2 \omega_g} L_{rp, \min} \quad (21)$$

Larger L_{rp} improves the frequency selection characteristics of the resonant tank, thereby reducing the harmonic currents in the high-frequency conversion stage. Thus, combining (20) and (21), the maximum of L_{rp} is adopted.

Furthermore, according to (18), C_{rp} is:

$$C_{rp} = \frac{1}{L_{rp} \omega_h^2} \quad (22)$$

The frequency of the switching harmonics can be or around the LC serial resonant frequency. R_r cannot be ignored when calculating the switching harmonic current. According to (3), I_{hs} is as follows:

$$I_{hs} = \sqrt{\sum_{\omega_y=0}^{\infty} \left[\frac{U_{arm,s}(\omega = \omega_y)}{Z_y} \right]^2} \leq \sigma_2 I_h = \frac{\sigma_2 \pi M P_L}{4 U_g}$$

$$Z_y = \sqrt{R_r^2 + \left(\omega_y L_{rp} - \frac{1}{\omega_y C_{rp}} \right)^2} \quad (23)$$

where $U_{arm,s}$ is the switching harmonics of U_{arm} . It is affected by the modulation method of the CFB stage, and in this work, $U_{arm,s}$ can be found in (46).

L_{rp} and C_{rp} can be determined by (21) and (22) because ω_g is already known, and ω_h is related to HFT. Thus, only the equivalent PWM switching frequency ω_s can be adjusted to satisfy the restriction in (23).

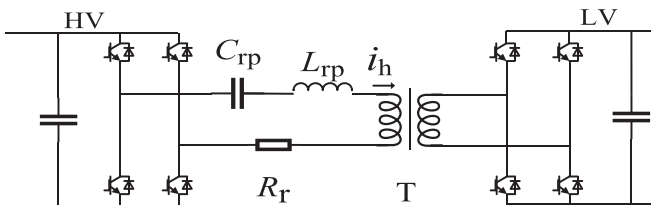


Fig. 4. Equivalent circuit of high frequency conversion stage.

The lower limit of ω_s can be obtained by taking $U_{arm,s}$ into (23).

Next, the analysis below considers the influence of the SM capacitor voltage ripple on i_h . The output voltage of the CFB bridge arm can be written as a sum of three parts:

$$u_{arm} = u_{arm,g} + u_{arm,h} + u_{arm,s} \quad (24)$$

Ignoring the switching harmonic current and considering the reference direction, as shown in Fig. 1b, the bridge arm current is the sum of two parts:

$$i_{arm} = i_g - i_h \quad (25)$$

According to (24) and (25), bridge arm charging power is:

$$P_{arm} = u_{arm} i_{arm} = (u_{arm,g} + u_{arm,h} + u_{arm,s})(i_g - i_h) =$$

$$(u_{arm,g} i_g - u_{arm,h} i_h) +$$

$$(-u_{arm,g} i_h + u_{arm,h} i_g + u_{arm,s} i_g - i_{arm,g} i_h) \quad (26)$$

The charging power of the bridge arm reflects the charging power of the SM capacitors. The high-frequency voltage ripple is small because the SM capacitor is a low-pass filter. According to the *Product to Sum Formula*: $u_{arm,g} i_g$ contains DC and double-line frequency components, and $u_{arm,h} i_h$ includes a DC component. Available from the power balance, the DC components of $u_{arm,g} i_g$ and $u_{arm,h} i_h$ are canceled by each other, and the double-line frequency component of $u_{arm,g} i_g$ is the same as that of the traditional CFB-type PET. Considering that $\omega_h \gg \omega_g$ and the bridge arm equivalent switching angular frequency ω_s satisfies $\omega_s \gg \omega_g$, $u_{arm,g} i_h$, $u_{arm,h} i_g$, and $u_{arm,s} i_g$ only contain high-frequency components.

To eliminate the low-frequency components of $u_{arm,s} i_h$, ω_s and ω_h should satisfy:

$$\omega_s - \omega_h \gg \omega_g \quad (27)$$

Once (27) is satisfied, the main voltage ripple of the SM capacitor in MFCC-PET is consistent with that of the traditional CFB type PET, and the method in [22] can be obtained to design the SM capacitor of MFCC-PET.

The voltage ripple of SM is mainly in double-line frequency. Assume its peak is $\sigma_4 U_{SM}$ ($\sigma_4 > 0$) and the peak of the modulation wave of the high-frequency square-modulation is 1 (unit). According to the *Fourier Transform*, the peak of the fundamental of a high-frequency square modulation wave is $4/\pi$ (unit). Furthermore, according to the *Product to Sum Formula*, when line frequency $f_g = 50$ Hz, the RMS of $f_h \pm 100$ Hz voltages, which are generated by the product of the SM capacitor double line-frequency ripple and high-frequency square modulation wave is:

$$U_{arm,SMh+} = U_{arm,SMh-} = \frac{1}{2} \frac{1}{\sqrt{2}} \frac{4}{\pi} \frac{N \sigma_4 U_{SM}}{2} = \frac{2 \sigma_4 U_g}{\pi M} \quad (28)$$

The RMS of the HFT injection harmonic current by $U_{arm,SMh+}$ and $U_{arm,SMh-}$ is:

$$\begin{cases} I_{h,SMh+} = \frac{2 \sigma_4 U_g}{\pi M \sqrt{R_r^2 + \left[2\pi(f_h + 100) L_{rp,x} - \frac{1}{2\pi(f_h + 100) C_{rp,x}} \right]^2}} \\ I_{h,SMh-} = \frac{2 \sigma_4 U_g}{\pi M \sqrt{R_r^2 + \left[2\pi(f_h - 100) L_{rp,x} - \frac{1}{2\pi(f_h - 100) C_{rp,x}} \right]^2}} \end{cases} \quad (29)$$

Available from (29), adjusting σ_4 to limit the HFT harmonic current is effective. When $U_g = 5.77$ kV, $f_g = 50$ Hz, $M = 0.75$, $3P_L = 1$ MW, $\sigma_1 = \sigma_2 = 3\%$, $f_h = 2.1$ kHz, $R_r = 0.01\%$ p.u., $\sigma_3 = \{15, 10, 5\}$, and $\sigma_4 = \{1\%, 2\%, 5\%, 10\%\}$, the ratios of the RMS of the sum of $i_{h,SMh+}$ and $i_{h,SMh-}$ to I_h are shown in Fig. 5.

Fig. 5 shows that the injection harmonic current accounts for a small amount when $\sigma_4 < 2\%$. The proportion of harmonic currents does not exceed 10% when $\sigma_4 = 5\%$, $\sigma_3 = 10$, or 15. The proportion of harmonic

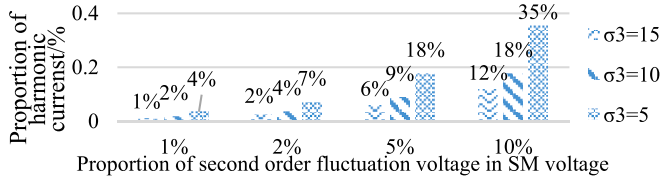


Fig. 5. Proportion of HFT harmonic currents generated by the 2nd order harmonic ripple of SM capacitor voltage under different σ_3 and σ_4 .

currents exceeds 10 % when $\sigma_4 = 10$ %. When $\sigma_4 \leq 5$ %, selecting the $U_r = 10U_g = 57.7$ kV is a balance of harmonic current and LC voltage stress.

The resonant voltage is extremely high, and the following methods can be used to reduce the LC voltage stress:

(a) Resonant inductor can be placed on the LV side;

(b) The HV side only keeps the necessary capacitance to satisfy design requirements (2), others can be placed on the LV side: According to (21), the minimum resonant inductance $L_{rp,min}$ required is $1/8.9$ of the selected inductance $L_{rp,max}$, in other words, to satisfy design requirement (2), the maximum resonance capacitance $C_{rp,max}$ is 8.9 times of the selected capacitance $C_{rp,min}$. Thus, it is only needed to retain $C_{rp,max}$ on the HV side. Thereby, the peak value of the resonance voltage across $C_{rp,max}$ is 57.7 kV/ $8.9 = 6.5$ kV, and its RMS is 4.6 kV. Considering the line-frequency phase voltage, the RMS voltage across $C_{rp,max}$ is 7.4 kV. An 8 kV high-frequency capacitor [23] is available for this application.

(c) Adopting the basic-function-unit cascade structure [20], the voltage stress of LC is inversely proportional to the number of cascaded basic function units.

In summary, the existence of an SM capacitor voltage ripple makes the resonant voltage of L_{rp} and C_{rp} the strictest condition for design. So, once σ_3 is determined by the manufacturing level of C_{rp} , from (1), L_{rp} and C_{rp} is acquired.

3. Modulation design

To achieve the mixed frequency conversion in section II, the NL-PWM is considered. First, to further reduce the voltage distortion of the traditional triangle carrier NL-PWM [24], in this section, a sawtooth carrier NL-PWM is proposed. Then, the implementation of mixed frequency conversion based on the proposed modulation method is studied.

3.1. Sawtooth carrier NL-PWM

For NL-PWM, one SM is in PWM state and the other SMs are in stair wave modulation state. Taking phase-a as an example, the stair wave voltage u_{stair} of CFB is:

$$u_{stair} = \begin{cases} U_{sm} \cdot \text{round}\left(\frac{u_{a,o}^*}{U_{sm}}\right), -N < \text{round}\left(\frac{u_{a,o}^*}{U_{sm}}\right) < N \\ U_{sm}(N-1), \text{round}\left(\frac{u_{a,o}^*}{U_{sm}}\right) \geq N \\ -U_{sm}(N-1), \text{round}\left(\frac{u_{a,o}^*}{U_{sm}}\right) \leq -N \end{cases} \quad (30)$$

Where $u_{a,o}^*$ is the phase-a reference voltage of CFB, it is a sin-wave voltage.

According to Fourier Series, the standardized spectrum of u_{stair} is:

$$\frac{u_{stair}}{U_{sm}} = -\frac{2}{n\pi} \sum_{n=1,3,5,\dots}^{\infty} \sum_{k=1}^{2N-2} \cos(ny_k) \sin(ny)$$

$$y_k = \begin{cases} \pi - \arcsin\left[\frac{\left(\frac{k}{N} - 1 + \frac{1}{2N}\right)}{M}\right], k = 1, 2, \dots, 2N-2 \\ 1.5\pi, k = 0 \\ 0.5\pi, k = 2N-1 \end{cases} \quad (31)$$

Where $\text{round}(x)$ is the rounding of x .

According to (30), Fig. 6 can be obtained.

Furthermore, the standardized phase-a PWM reference is:

$$\frac{u_{PWM,a}^*}{U_{sm}} = \frac{u_{a,o}^*}{U_{sm}} - \frac{u_{stair}}{U_{sm}} \quad (32)$$

The circuit of full bridge SM is shown in Fig. 7.

Based on the sawtooth carrier and unipolar modulation, for one SM, the PWM reference voltage, the carrier, and the SM output voltage are shown in Fig. 8.

According to Fig. 8:

$$u_{n1,oi}(x) = \begin{cases} U_{sm}x \in [\theta - \pi\pi) \\ 0x \in [0\theta - \pi) \cup [\pi 2\pi) \end{cases} \quad (33)$$

$$u_{p1,oi}(x) = \begin{cases} U_{sm}x \in [0\theta) \\ 0x \in [\theta 2\pi) \end{cases} \quad (34)$$

$$\frac{u_{PWM}^*}{N} = u_{p1,n1}(x) = u_{p1,oi}(x) - u_{n1,oi}(x) \quad (35)$$

$$\theta = \pi(MNsiny + N - 1 - k), k = 0, 1, 2, \dots, 2N-1 \quad (36)$$

The double Fourier Series is [25]:

$$u(t) = u(x, y) = \frac{A_{00}}{2} + \sum_{n=1}^{\infty} [A_{0n} \cos(ny) + B_{0n} \sin(ny)] +$$

$$\sum_{m=1}^{\infty} [A_{m0} \cos(mx) + B_{m0} \sin(mx)] +$$

$$\sum_{m=1}^{\infty} \sum_{n=\pm 1}^{\pm \infty} [A_{mn} \cos(mx + ny) + B_{mn} \sin(mx + ny)]$$

$$A_{mn} + jB_{mn} = \frac{1}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\pi}^{\pi} u(x, y) e^{j(mx+ny)} dx dy \quad (37)$$

According to (37), for the PWM voltage of CFB, the Fourier Coefficients are:

$$\frac{A_{00}}{U_{sm}} = 0 \quad (38)$$

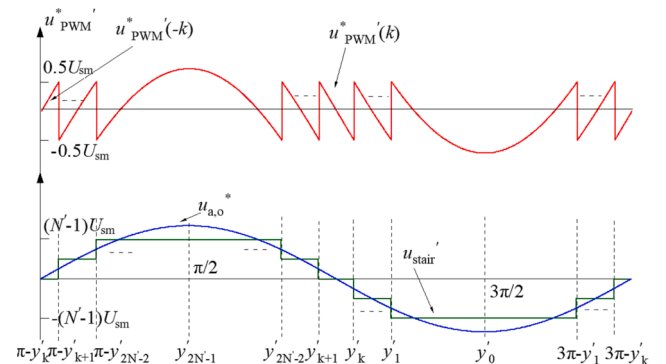


Fig. 6. Bridge-arm modulation voltage, SM PWM reference voltage, and bridge-arm stair wave voltage.

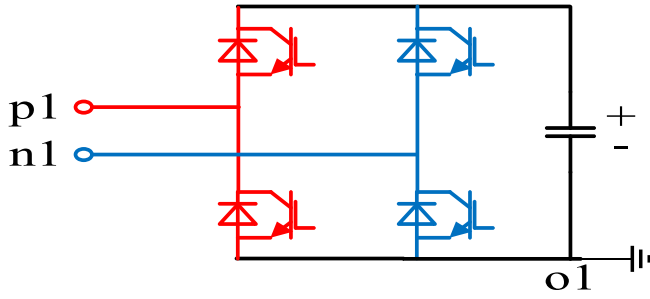


Fig. 7. Circuit of full-bridge SM.

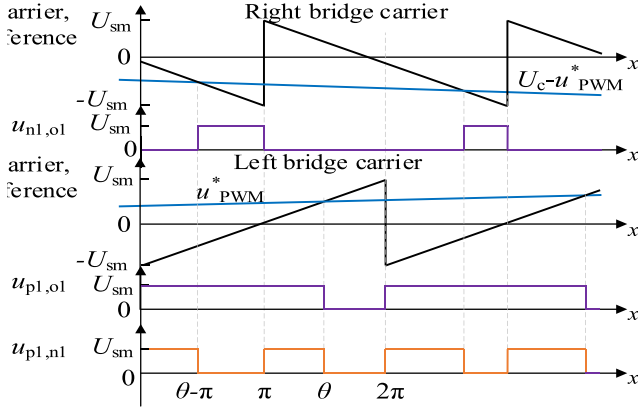


Fig. 8. PWM carrier and the reference voltage of upper and lower bridge arms.

$$\frac{A_{0n}}{U_{sm}} = 0, n \neq 0 \quad (39)$$

$$A_{mn} = 0, m \neq 0 \quad (40)$$

$$\frac{B_{00}}{U_{sm}} = 0 \quad (41)$$

$$\frac{B_{01}}{U_{sm}} = MN + \frac{2}{\pi} \sum_{k=1}^{2N-2} \cos y_k \quad (42)$$

$$\frac{B_{0n}}{U_{sm}} = \frac{2}{n\pi} \sum_{k=1}^{2N-2} \cos(ny_k), n = 3, 5, 7 \dots \quad (43)$$

$$B_{mn} =$$

$$\begin{cases} \frac{(-1)^{mN+1}}{0.5\pi m} \sum_{i=2,4,6\dots}^{\infty, i=\pm n} J_i(m\pi MN), m \neq 0, n = \pm 2, \pm 4, \pm 6 \dots \\ \frac{2}{\pi m} [1 - (-1)^{mN} J_0(m\pi MN)], m \neq 0, n = 0 \end{cases} \quad (44)$$

Taking (38)~(44) into (37), the *Fourier Series* of the CFB PWM voltage is:

$$\begin{aligned} u_{\text{PWM,a}}^* &= \frac{2U_c}{n\pi} \sum_{n=1,3,5\dots}^{\infty} \sum_{k=1}^{2N-2} \cos(ny_k) \sin(ny) + \\ &MN U_{sm} \sin(\omega_r t) + 2U_{sm} \sum_{m=2,4,6\dots}^{\infty} B_{m0} \sin(m\omega_c t) + \\ &2U_{sm} \sum_{m=2,4,6\dots}^{\infty} \sum_{n=\pm 1}^{\pm \infty} B_{mn} \sin(m\omega_c t + n\omega_r t) \end{aligned} \quad (45)$$

Summing (31) and (45), the *Fourier Series* of CFB bridge arm voltage is:

$$\begin{aligned} u_{ao} &= MN U_{sm} \sin(\omega_r t) + U_{arm,s} = \\ &MN U_{sm} \sin(\omega_r t) + 2U_{sm} \sum_{m=2,4,6\dots}^{\infty} B_{m0} \sin(m\omega_c t) + \\ &2U_{sm} \sum_{m=2,4,6\dots}^{\infty} \sum_{n=\pm 1}^{\pm \infty} B_{mn} \sin(m\omega_c t + n\omega_r t) \end{aligned} \quad (46)$$

Furthermore, the *Fourier Series* of the ab line voltage is:

$$\begin{aligned} u_{ab} &= \sqrt{3} MN U_{sm} \cos\left(\omega_r t - \frac{\pi}{3}\right) + \\ &4U_{sm} \sum_{m=2,4,6\dots}^{\infty} \sum_{\substack{n=\pm 1, \pm 2, \pm 4 \dots \\ n \neq 3r, r \in \mathbb{Z}}}^{\pm \infty} B_{mn} \times \\ &\cos\left(m\omega_c t + n\omega_r t - n\frac{\pi}{3}\right) \sin\left(n\frac{\pi}{3}\right) \end{aligned} \quad (47)$$

Taking $N = 12$, $M = 0.75$, and $\omega_c/\omega_r = 60$ as an example [24], according to (47) and [24], the line voltage spectrums of CFB based on the sawtooth carrier NL-PWM and the triangular carrier NL-PWM under unipolar modulation are shown in Fig. 9(a) and (b), respectively. Although the sawtooth carrier NL-PWM has more abundant sidebands than the triangular carrier one, the amplitude of sidebands is lower, and the THDu (2nd–250th) is reduced by 24.2%. The simulation results in Section IV prove that the sawtooth carrier NL-PWM has a better quality of line current than the triangular carrier.

For SM voltage balancing, NL-PWM uses the sorted method [26]. The bridge arm current of MFCC-PET contains mixed-frequency components. The criterion of voltage balancing is unique:

Taking $i_g > 0$ as an example, assume that the output voltage level of SM is Sw , $Sw = 1$ refers to the positive voltage level, $Sw = 0$ refers to the zero voltage level, and $Sw = -1$ refers to a negative voltage level. In one $T_h/2$, the low-frequency current in the bridge arm can be regarded as a constant because $T_h/2 \ll T_g$. According to the reference direction shown in Fig. 1b, assuming that voltage balancing is conducted at $t = 0$, then for every $T_h/2$, the change of SM capacitor charge:

$$\Delta Q_{\text{nonPWM}} = Sw \int_0^{T_h/2} (i_g - i_h) dt \quad (48)$$

According to (48), ΔQ_{nonPWM} is determined by the integration of Sw and $i_g - i_h$ between $t = 0$ and $t = T_h/2$. Therefore, the sign of the above integration should be judged first. Then, the suitable Sw should be selected.

Assuming the above integration to 0:

$$\frac{T_h}{2} i_g - \int_0^{T_h/2} i_h dt = 0 \quad \text{That is: } |i_g| = \frac{2\sqrt{2}I_h}{\pi} = I_{ge} \quad (49)$$

Available from (48) and (49), when $|i_g| = I_{ge}$, $\Delta Q_{\text{nonPWM}} = 0$; when $|i_g| > I_{ge}$, ΔQ_{nonPWM} and $i_g Sw$ share the same sign; When $|i_g| < I_{ge}$, ΔQ_{nonPWM} and $-i_h Sw$ share the same sign.

According to the above analysis, the specific voltage balancing method is as follows:

When $|i_g| < I_{ge}$ and $-i_h < 0$, or $|i_g| \geq I_{ge}$ and $i_g < 0$: If $u_{\text{PWM}}^* \geq 0$, the SMs

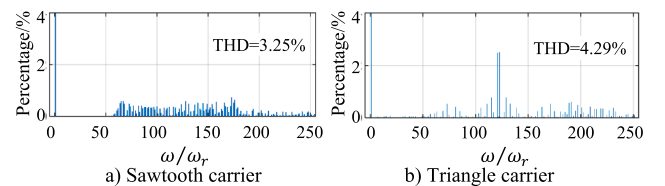


Fig. 9. Spectrum of the line voltage of NL-PWM.

of the capacitor voltage from high to low in turn output: positive voltage level (+), PWM, zero voltage level (0), and negative voltage level (-); If $u_{PWM}^* < 0$, the capacitor voltage from high to low in turn output: +, 0, PWM, and -;

When $|i_g| < I_{ge}$ and $-i_h \geq 0$, or $|i_g| \geq I_{ge}$ and $i_g \geq 0$: If $u_{PWM}^* \geq 0$, the SMs of the capacitor voltage from high to low in turn output: -, 0, PWM, and +; If $u_{PWM}^* < 0$, the SMs of the capacitor voltage from high to low in turn output: -, PWM, 0, and +.

The above analysis does not consider the PWM SM. The change of its charge has a minimal influence on the change of the bridge arm charge because of only one PWM SM.

3.2. Implementation of mixed frequency conversion

To meet the requirements of mixed frequency modulation, NL-PWM needs to simultaneously output three types of voltage: high-frequency rectangular wave voltage, quasi-sinusoidal step wave voltage, and PWM voltage. Due to the use of unipolar frequency modulation, both the quasi-sinusoidal step wave voltage and PWM voltage are unipolar voltages. However, to improve the utilization of DC voltage, high-frequency rectangular wave voltage is bipolar voltage. Suppose high-frequency rectangular waves are directly superimposed on the bridge arm output of CHB. In that case, it will cause significant power backflow due to the difference in positive and negative levels of the submodules. Therefore, it is necessary to sum the high-frequency rectangular wave modulation voltage with the quasi-sinusoidal step-wave modulation voltage to obtain the total output level. Then, calculate the number of sub-modules that need to be input and bypassed to achieve positive and negative level cancellation.

The voltage balancing method is similar to the process described in Section III A. Still, considering that there are a large number of sub-modules outputting high-frequency rectangular wave voltage and only one submodule outputting PWM voltage, in order to reduce the additional switching frequency generated by voltage sharing switching, the voltage sharing switching time is set at the rising and falling edges of the high-frequency rectangular wave.

4. Simulation verification

Simulation verifications are carried out by EMTDC/PSCAD. The simulation model is shown in Fig. 1b. The HV sides and LV sides of PET are connected to the 10 kV network and 0.75 kV LVDC loads, respectively. The parameters of the simulation model are shown in Table 1.

Simulation results of grid voltage and current with triangular carrier and sawtooth carrier NL-PWM under-rated power is shown in Fig. 10(a) and (b), respectively. The three-phase voltage and current are in phase, realizing unit factor control. In Fig. 10(a), THDi (2nd–39th) is 1.31 %, and THDi (2nd–250th) is 1.72 %. In Fig. 10(b), THDi (2nd–39th) is 1.19 %, and THDi (2nd–250th) is 1.57 %, indicating that THDi is reduced by 9.2 % and 8.7 %, respectively, by adopting the sawtooth carrier NL-PWM.

Simulation results of the CFB bridge arm current and the LVDC voltage are shown in Fig. 11. The bridge arm current contains line-

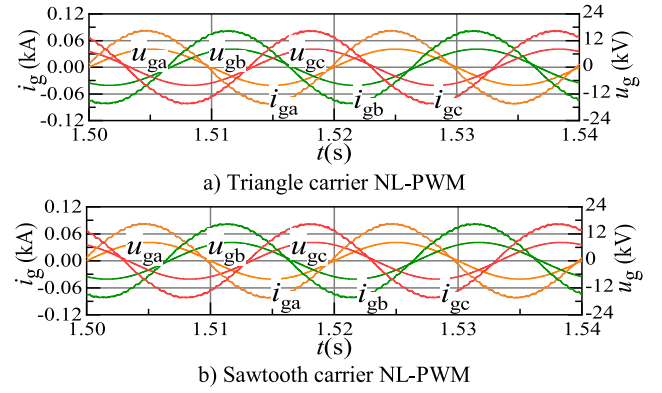


Fig. 10. Waveform of grid-side voltage and current.

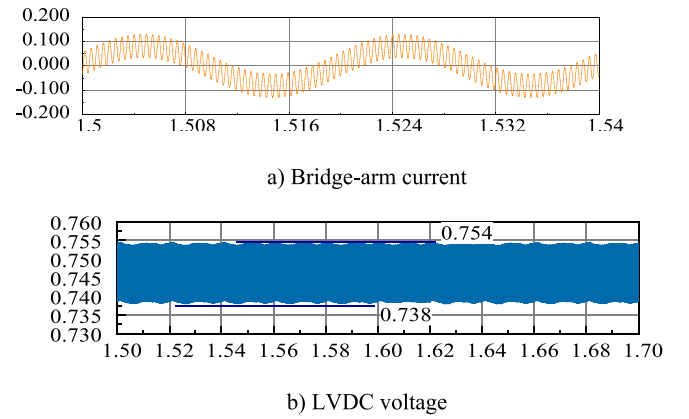


Fig. 11. Waveform of bridge-arm current and LVDC voltage.

frequency components and high-frequency components, which is in accordance with theoretical analysis. The RMS current is 62 A, which has a small difference from the theoretical value of 67.1 A by (11). The ripple of LVDC voltage is less than 1.07 %.

The simulation results of the voltage and its dispersion of the 24 SMs of the CFB bridge arm under rated load are shown in Fig. 12. The maximum dispersion of SM voltage is 18 V (2 %), indicating good voltage balancing. The SM capacitance is 1,375 μ F, and the peak ratio of the SM voltage second-order ripple is 2 %, which is equal to CFB-PET [22]. Fig. 12(d) shows that when $t = 1.6$ s, power reverses, and the SM voltage reaches a steady state 0.8 s later. During the whole process, the SM voltages are well balanced, which verifies that the proposed control can ensure the voltage balancing of SM.

Simulation results of grid current, HFT LV-side current, and LVDC voltage when load drops from 1 MW to 0.8 MW are shown in Fig. 13. When $t = 1.6$ s, load drops 0.2p.u., and only after 0.3 s, steady state is obtained.

The line voltage spectrum of sawtooth carrier and triangular carrier NL-PWMs are shown in Fig. 14(a) and (b), respectively. Comparison of Figs. 14 and 8 shows that the theoretical analysis and simulation results agree. The THDu (2nd–255th) of the sawtooth carrier NL-PWM is 24.2 % lower than that of the triangular carrier one.

5. Experimental verification

The experimental setup is shown in Fig. 15. The experiment verification is conducted according to the prototype parameters in Table 2.

The experimental results of the HV-side AC voltage, current, and LVDC voltage under rated load are shown in Fig. 16. The voltage and current are in phase. The AC voltage contains a small amount of high-

Table 1
Simulation Parameters of MFCC-PET.

Rated power P_N / kW	Line voltage U_{gl} /kV	Line frequency f_g /Hz	Standardized filter inductor L_f /p.u.
1000	10	50	0.05
Rated voltage of SM U_{SM} /V	Number of SMs per phase N	Resonant inductor L_{rp} /mH	Resonant capacitor C_{rp} /nF
900	24	84	68.4
Frequency of HFT f_h /Hz	PWM carrier frequency f_c /Hz	Ratio of HFT n	LVDC voltage U_{dc} /V
2100	3000	10.8:0.75	750

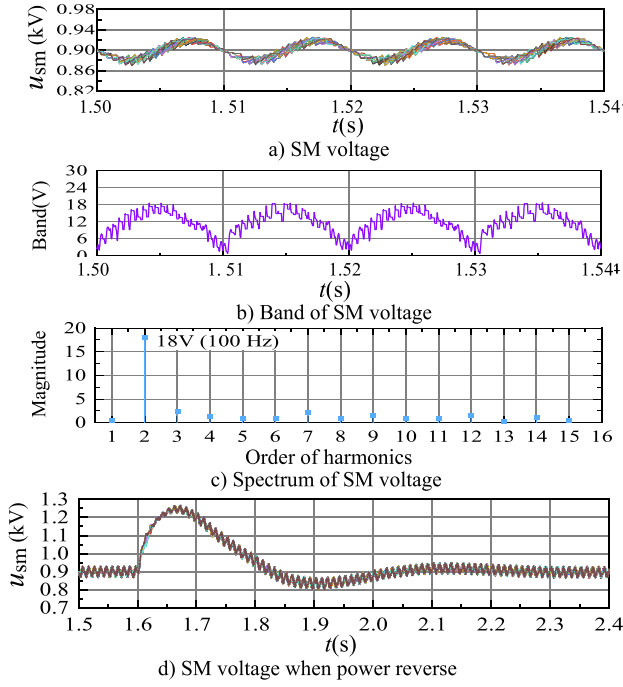


Fig. 12. Waveform of SM voltages.

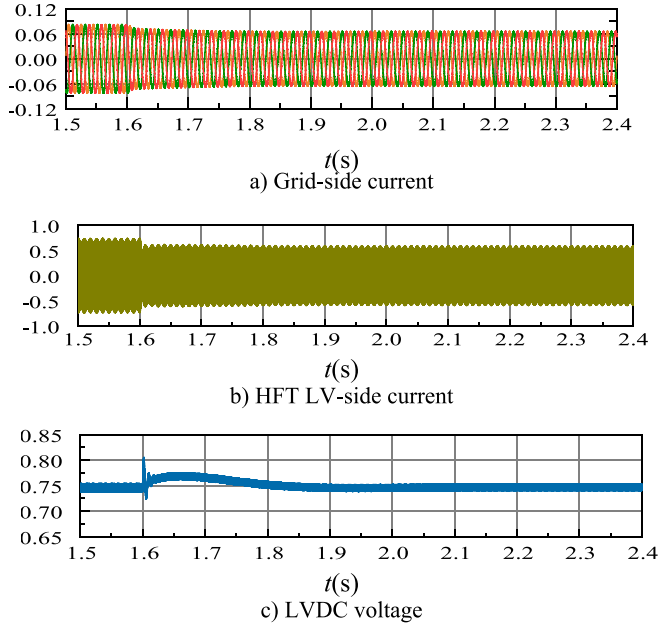


Fig. 13. Waveform of grid-side current, HFT LV-side current and LVDC voltage while load drops from 1 MW to 0.8 MW.

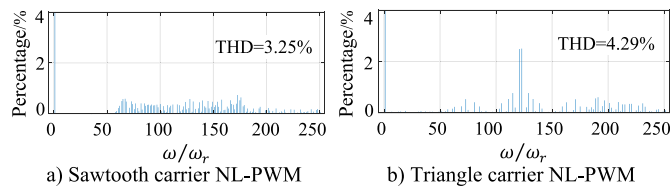


Fig. 14. Spectrum of line voltage.



Fig. 15. Experimental device.

Table 2
MFCC-PET Prototype Parameters.

Rated power P_N / kW	Line voltage U_{gl}/V	Line frequency f_g/Hz	Filter inductor L_f / mH
2	100	50	1.6
Rated voltage of SM U_{SM}/V	Number of SMs per phase N	Resonant inductor $L_{rp}/\mu H$	Resonant capacitor $C_{rp}/\mu F$
52	4	500	12
HFT frequency f_h / Hz	Carrier frequency f_c/Hz	Ratio of HFT n	LVDC voltage U_{dc}/V
3000	3000	1.2:1	80

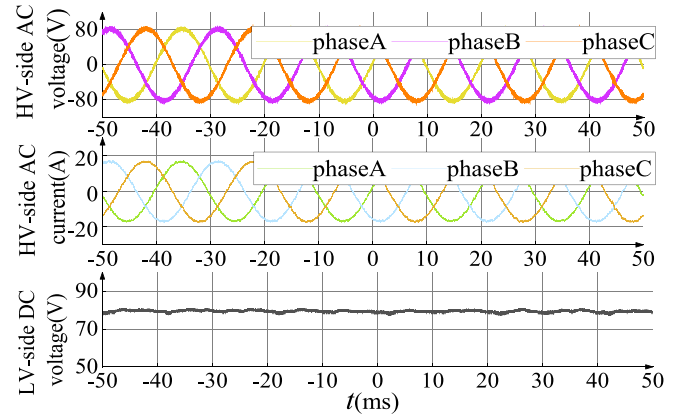


Fig. 16. Experiment waveforms of the inputs and outputs of PET.

order harmonics because the network is formed by a Chroma power source, which has an internal impedance. The THDi (2nd–39th) is only 1.52 %. The LVDC voltage is 80 V, which is consistent with the rated value, and the voltage ripple is very small.

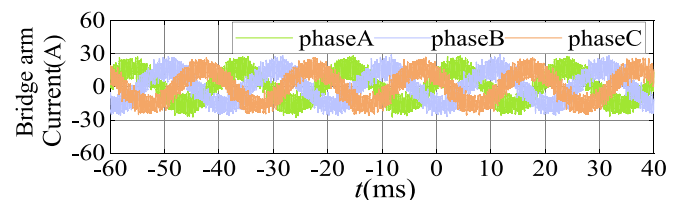


Fig. 17. Experiment waveforms of the bridge-arm current.

The experimental results of HV-side three-phase bridge arm currents are shown in Fig. 17. The bridge arm current contains low-frequency components and high-frequency components, reflecting the characteristics of the mixed-frequency conversion.

The experimental results of HFT secondary side voltage and current are shown in Fig. 18. The voltage and current are almost in phase. By Fourier Transform, standardizing the current shown in Fig. 19(a) by the magnitude of 3 kHz component, the spectrum is shown in Fig. 19. According to Fig. 19, except for the 3 kHz component, the amplitude of the other components is small. The amplitude of the 50 Hz component is about 3.2 %, which has a small difference with the design value 3.09 %. The total content of the PWM harmonic current and the harmonic current caused by the SM voltage ripple is 13.2 %, and its error from the design value of 11.5 % is reasonable. The resonance voltage for the prototype is $2U_g$, and harmonic currents can be further reduced by increasing the resonance voltage.

The experimental results of the voltages of the four SMs of the CFB bridge arm are shown in Fig. 20. The voltages of the four SMs are well-balanced. The standardized spectrum of SM capacitor voltage is shown in Fig. 21. Voltage is standardized by the DC component. The SM voltage ripple is mainly in double-line frequency, and its amplitude is 3.6 %, which is slightly less than the theoretical value of 3.8 %.

The experimental results of PWM voltage of CFB, three-phase AC currents, and LVDC voltage when load steps up from 1,000 W to 2,000 W are shown in Fig. 22. The results based on sawtooth carrier NL-PWM and triangular carrier NL-PWM are shown in Fig. 22 a) and b), respectively. Load steps up at $t = -37$ ms. During the dynamic process, the AC current is not distorted and reaches a steady state after three line-frequency periods. During the dynamic process, a drop of 8 V (0.1p.u.) occurs in the LVDC voltage, and the LVDC voltage restores the rated value after three line-frequency periods. The results show that MFCC-PET can handle the dynamic state.

The spectrum of steady-state current in Fig. 22 is shown in Fig. 23. The voltage is standardized by the magnitude of 50 Hz component. Comparing Fig. 23(a) and (b), the sawtooth carrier NL-PWM has a smaller amount of current harmonic than the triangular one, especially the high-order harmonic. Fig. 23(a) and (b) show that THDi (2nd–39th) are 1.52 % and 1.82 % respectively, indicating that sawtooth carrier NL-PWM has 16.5 % less THDi than the triangular carrier. The THDi (2nd–300th) are 2.16 % and 2.46 % respectively. The THDi of sawtooth carrier one is 12.2 % less than the triangular one.

The experimental results of the capacitor voltage of the four SMs of the phase a CFB bridge arm when the load drops from 2 kW to 1 kW are shown in Fig. 24. The LVDC load drops at $t = -20$ ms. The voltages of the four SMs are well-balanced during the whole dynamic process.

The above experimental results show that the topology and control of MFCC-PET have good input and output quality as well as dynamic and steady-state performance.

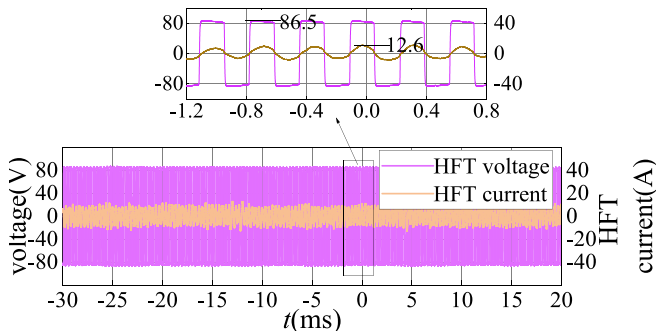


Fig. 18. Experiment waveforms of the voltage and current of HFT.

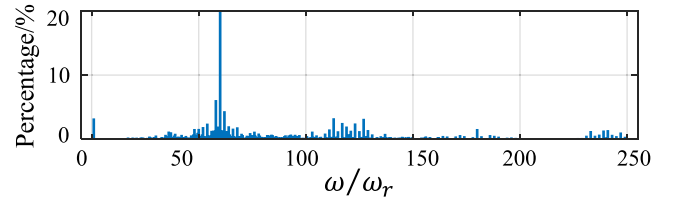


Fig. 19. Spectrum of HFT current.

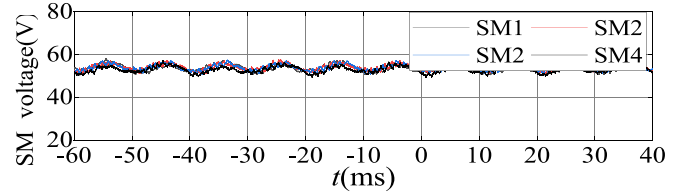


Fig. 20. Experiment waveforms of bridge-arm SM voltages of CFB.

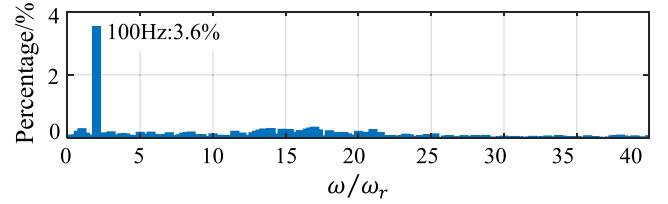


Fig. 21. Spectrum of SM voltage.

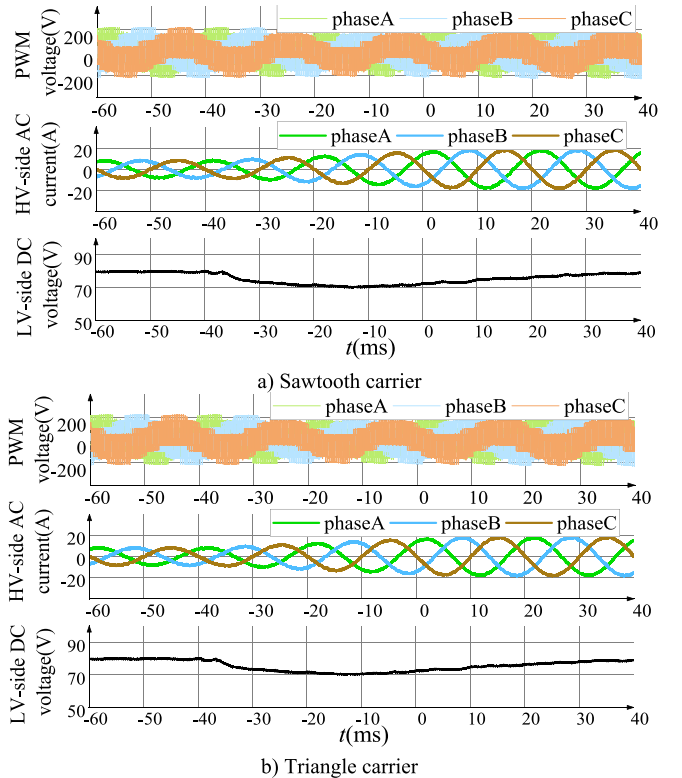


Fig. 22. Experiment waveforms of PET input and output when loads step up.

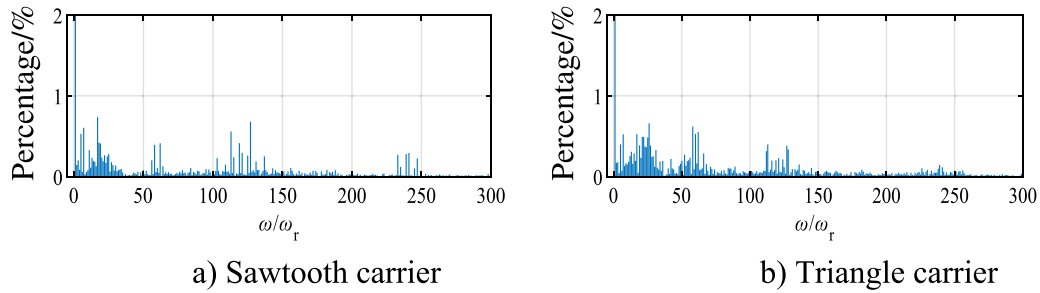


Fig. 23. Spectrum of AC current.

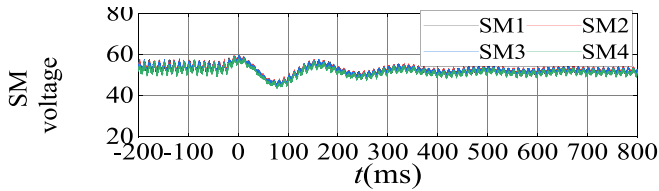


Fig. 24. Experiment waveforms of four SM voltages of the phase a CFB bridge arm when load drops 0.5p.u.

6. Conclusion

MFCC-PET has characteristics such as low cost and compact structure. This work aims to design MFCC-PET. A comprehensive design of circuit parameters is proposed, laying the foundation for the stable, reliable operation of MFCC-PET. A sawtooth carrier NL-PWM is proposed. This modulation effectively reduces the line voltage THD compared with the existing triangular carrier NL-PWM and obtains a high-quality line current. Based on the proposed modulation, the implementation of mixed-frequency conversion is studied, and an SM voltage balancing method that can function well under the mixed-frequency bridge-arm currents is proposed. A 100 V/2,000 W prototype is established and successfully placed into operation based on the above studies, verifying the feasibility of MFCC-PET.

Funding

This work was supported by State Key Laboratory of Alternate Electrical Power System with Renewable Energy Sources (North China Electric Power University) under Grant LAPS2021-24.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

References

- [1] Hannan MA, et al. State of the art of solid-state transformers: advanced topologies, implementation issues, recent progress and improvements. *IEEE Access* 2020;8: 19113–32.
- [2] Manjrekar MD, Kieferndorf R, Venkataramanan G. Power electronic transformers for utility applications. In: Conference Record of the 2000 IEEE Industry Applications. Thirty-Fifth IAS annual meeting and world conference on industrial applications of electrical energy (Cat. No.00CH37129), Rome, Italy; 2000. p. 2496–2502, vol.4.
- [3] Chen H, Divan D. Soft-switching solid-state transformer (S4T). *IEEE Trans Power Electron* 2018;33(4):2933–47.
- [4] Hugo N, Stefanutti P, Pellerin M, Akdag A. Power electronics traction transformer. In: 2007 European conference on power electronics and applications, Aalborg; 2007. p. 1–10.
- [5] Sabahi M, Hosseini SH, Sharifian MB, Goharizi AY, Gharehpetian GB. Zero-voltage switching bi-directional power electronic transformer. *IET Power Electron* 2010;3 (5):818–28.
- [6] Huber JE, Böhrer J, Rothmund D, Kolar JW. Analysis and cell-level experimental verification of a 25 kW all-SiC isolated front end 6.6 kV/400 V AC-DC solid-state transformer. *CPSS Trans Power Electron Appl* 2017;2(2):140–8.
- [7] Giacomuzzi S, Langwasser M, De Carne G, Buja G, Liserre M. Smart transformer-based medium voltage grid support by means of active power control. *CES Trans Electr Mach Syst* 2020;4(4):285–94.
- [8] Zhao X, et al. DC solid state transformer based on three-level power module for interconnecting MV and LV DC distribution systems. *IEEE Trans Power Electron* 2021;36(2):1563–77.
- [9] Zhang L, Qin J, Zou Y, Duan Q, Sheng W. Analysis of capacitor charging characteristics and low-frequency ripple mitigation by two new voltage-balancing strategies for MMC-Based solid-state transformers. *IEEE Trans Power Electron* 2021;36(1):1004–17.
- [10] Wang Y, et al. A dual-active-bridge with half-bridge submodules DC solid-state transformer for DC distribution networks. *IEEE J Emerg Select Top Power Electron* 2021;9(2):1891–904.
- [11] Zhang X, Xu Y, Siddique A, Long Y, Xiao X. A microprocessor resource-saving dual active bridge control for startup and restart of three-stage modular solid-state transformer. *IEEE Trans Power Delivery* 2020;35(3):1443–54.
- [12] Li K, et al. Design and implementation of four-port megawatt-level high-frequency-bus based power electronic transformer. *IEEE Trans Power Electron* 2021;36(6): 6429–42.
- [13] Ma D, Chen W, Shu L, Qu X, Hou K. A MMC-based multiport power electronic transformer with shared medium-frequency transformer. *IEEE Trans Circ Syst Exp Briefs* 2021;68(2):727–31.
- [14] Huber JE, Kolar JW. Applicability of solid-state transformers in today's and future distribution grids. *IEEE Trans Smart Grid* 2019;10(1):317–26.
- [15] Zheng L, Kandula RP, Divan D. Soft-switching solid-state transformer with reduced conduction loss. *IEEE Trans Power Electron* 2021;36(5):5236–49.
- [16] Zhao T, et al. Module power balance control and redundancy design analysis of cascaded PV solid-state transformer under fault conditions. *IEEE J Emerg Select Top Power Electron* 2021;9(1):677–88.
- [17] Huber JE, Kolar JW. Volume/weight/cost comparison of a 1MVA 10 kV/400 V solid-state against a conventional low-frequency distribution transformer. In: 2014 IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburgh, PA; 2014. p. 4545–4552.
- [18] FF225R17ME4[EB/OL]. https://www.infineon.com/dgdl/Infineon-FF225R17ME4-DS-v02_04-EN.pdf?fileId=db3a30431ddc9372011e1c4df9f53c3d.
- [19] FF600R17ME4[EB/OL]. https://www.infineon.com/dgdl/Infineon-FF600R17ME4-DS-v03_00-EN.pdf?fileId=db3a304333b8a7ca0133c67bfb6d6156.
- [20] Zhang X, Xu Y, Long Y, Xu S, Siddique A. Hybrid-frequency cascaded full-bridge solid-state transformer. *IEEE Access* 2019;7:22118–32.
- [21] Shu L, Chen W, Zhang C. Power electronic transformer based on mixed-frequency modulation strategy. In: 2019 10th International conference on power electronics and ECCE Asia (ICPE 2019 - ECCE Asia), Busan, Korea (South); 2019. p. 1559–64.
- [22] Sau S, Fernandes BG. Theoretical analysis and comparison of capacitor requirement in modular converters for grid integration of high power solar PV. In: 2019 IEEE Energy Conversion Congress and Exposition (ECCE), Baltimore, MD, USA; 2019. p. 5514–5521.
- [23] DAWNCAP[EB/OL]. <http://www.dawn-cap.cn/upload/201609/DAWNCAP-DGR%202015.pdf>.
- [24] Ding K, Cheng KWE, Zou YP. Analysis of an asymmetric modulation method for cascaded multilevel inverters. *IET Power Electron* 2012;5(1):74–85.
- [25] Li Y, Wang Y, Li BQ. Generalized theory of phase-shifted carrier PWM for Cascaded H-bridge converters and modular multilevel converters. *IEEE J Emerg Select Top Power Electron* 2016;4(2):589–605.
- [26] Wang Y, Hu C, Ding R, Xu L, Fu C, Yang E. A nearest level PWM Method for the MMC in DC distribution grids. *IEEE Trans Power Electron* 2018;33(11):9209–18.
- [27] Yue YQY et al. 'Comprehensive power losses model for electronic power transformer. *IEEE Access* 2018;vol. 6. p. 14926–14934.

Yonghai Xu received the B.S. degree from Tsinghua University, Beijing, China, the M.S. and Ph.D. degrees in power system and its automation from North China Electric Power University (NCEPU), Beijing, China, in 1989, 1992, and 2002, respectively. He is currently

a Professor with the School of Electrical and Electronic Engineering, NCEPU. His research interests include power quality analysis and control, and new energy power system.

Xueyin Zhang received the B.S. degree in smart grid information engineering and the Ph.D. degree in electrical engineering from North China Electric Power University (NCEPU), Beijing, China, in 2015 and 2020, respectively. From 2018 to 2019, he was a Ph.D. Visiting Scholar with FREEDM System Center, North Carolina State University, NC, USA. From 2020 to 2022, he was with the Nanjing NR Electric Co. Ltd., Nanjing, China. Since 2022, he has been with the Tsinghua Sichuan Energy Internet Research Institute, Chengdu, China. His research interests include multilevel converter and solid-state transformer

XU DONG received the B.S. degree in electrical engineering and automation from the Shandong University of Technology, Zibo, China, and the M.S. degree in electrical engineering in North China Electric Power University (NCEPU), Beijing, China in 2019 and 2022, respectively. Since 2022, he has been with the Jinan power supply company, Jinan, China. His research interest includes power quality and solid-state transformer.

Abubakar Siddique was born in Lodhran (Punjab), Pakistan. He received his Ph.D. degree from North China Electric Power University (NCEPU) Beijing, China in 2019 and his Masters and Bachelor's degrees from Islamia University Bahawalpur (IUB), Punjab, Pakistan in 2011 and 2013 respectively. Dr. Abubakar Siddique is currently working as an assistant professor in Electrical Engineering Department at Khwaja Fareed University of

Engineering & Information Technology (KFUEIT) Punjab, Pakistan. He has also worked at Islamia University Bahawalpur (IUB) Pakistan as lecturer. He is a professional member of the IEEE organization NJ, USA, member of IEEE Pakistan, and a member of The Institution of Engineers Pakistan (IEP). Further, he is also a life member of the Pakistan Engineering Council. He is an author and co-author of many highly indexed Journals and a potential reviewer of many papers in ISI, Scopus, and Conference proceeding Journals. Abubakar was awarded a fully funded doctoral scholarship from government of China. His research interests include Advanced Dielectric Materials and High Voltage insulating Testing Technology, perovskite solar cell (PSC) technology, and power quality control in electric power distribution systems.

Dr. Waseem Aslam was born in Muzaffargarh, Pakistan. He received the BSc. and MSc. degrees from UCET, Islamia University of Bahawalpur, Punjab, Pakistan in 2011 and 2013, respectively, all in Electrical Engineering (Power). He received PhD degree in Electrical Engineering (Power) from North China Electric Power University (NCEPU) Beijing, China in 2019. Currently, he is working as an Assistant Professor in the Department of Electrical Engineering, University of Sargodha (UOS) Sargodha, a major public sector University in Punjab, Pakistan. He is the author and co-author of many publications in international journals and conference proceedings in the area of the power system and power electronics. His research interests include power quality improvement, renewable energy, smart grids, high voltage, reliability and power electronics.