

SULIT



**BAHAGIAN PEPERIKSAAN DAN PENILAIAN
JABATAN PENDIDIKAN POLITEKNIK
KEMENTERIAN PENDIDIKAN TINGGI**

JABATAN KEJURUTERAAN MEKANIKAL

PEPERIKSAAN AKHIR

SESI JUN 2017

DJM3063 : DIGITAL SYSTEM

TARIKH : 31 OKTOBER 2017

MASA : 2.30 PETANG - 4.30 PETANG (2 JAM)

Kertas ini mengandungi **SEPULUH (10)** halaman bercetak.

Struktur (4 soalan)

Dokumen sokongan yang disertakan : Tiada

JANGAN BUKA KERTAS SOALAN INI SEHINGGA DIARAHKAN

(CLO yang tertera hanya sebagai rujukan)

SULIT

INSTRUCTION:

This section consists of **FOUR (4)** structured questions. Answer **ALL** questions.

ARAHAN:

Bahagian ini mengandungi EMPAT (4) soalan struktur. Jawab SEMUA soalan.

QUESTION 1**SOALAN 1**

CLO1
C1

(a) Write the following numbers to the number system required (display clear calculation).

- i. 1111010101.11_2 to hexadecimal number
- ii. 745.23_8 to decimal number

Tuliskan nombor berikut ke sistem nombor yang diperlukan (tunjukkan jalan kira dengan jelas):

- i. 1111010101.11_2 ke nombor heksadesimal
- ii. 745.23_8 ke nombor desimal

[5 marks]

[5 markah]

CLO1
C2

(b)

- i. Identify the Boolean expression for three input Ex- Or (X-OR) gate.
- ii. Draw the gate and the truth table.

- i. *Kenalpasti persamaan Boolean bagi tiga masukan get Eks-Atau (EX-ATAU).*
- ii. *Lukiskan get tersebut dan jadual kebenaran.*

[6 marks]

[6 markah]

CLO1
C3

- (c) Given the expression $X = \overline{A}BC + \overline{A}\overline{B}\overline{C} + ABC + A\overline{B}C + A\overline{B}\overline{C}$. Draw the circuit. Then simplify the expression by using the Karnaugh's Map.

Diberi persamaan $X = \overline{A}BC + \overline{A}\overline{B}\overline{C} + ABC + A\overline{B}C + A\overline{B}\overline{C}$. Lukiskan litar tersebut. Kemudian dengan menggunakan Peta Karnaugh permudahkan persamaan tersebut.

[8 marks]

[8 markah]

CLO1
C4

- (d) Solve the following calculations by using 2's complement method.

Selesaikan pengiraan berikut dengan menggunakan kaedah Pelengkap 2.

- (i) $48 - 23$
- (ii) $-48 - 23$
- (iii) $23 - 48$

[6 marks]

[6 markah]

QUESTION 2
SOALAN 2CLO1
C1

- (a) For active high SR flip-flop:
- Draw the logic symbol.
 - Show the truth table.

Flip-flop SR aktif tinggi:

- Lukiskan simbol logik.*
- Tunjukkan jadual kebenaran*

[5 marks]

[5 markah]

CLO1
C2

- (b) The JK flip-flop can be develop by these two flip-flops. Differentiate the logic circuit by using:
- D flip-flop.
 - T flip-flop.

Flip-flop JK boleh dibina daripada dua jenis flip-flop di bawah. Bandingkan litar logik dengan menggunakan:

- Flip-flop D.*
- Flip-flop T.*

[6 marks]

[6 markah]

(c) Complete the timing diagram in Figure 2 (c) for the negative edge triggering active high clocked SR flip-flop by assuming the initial conditions Q is '0'.

The timing diagram shows four signals over time:

- Clk**: A periodic square wave clock signal.
- S**: The Set input, which is high for the first two clock cycles, low for the next three, high for one, low for two, and high for one.
- R**: The Reset input, which is low for the first two clock cycles, high for one, low for two, high for one, and low for the last two.
- Q**: The output signal, which starts low and changes state at each clock edge based on the S and R inputs. It becomes high when S is high and R is low, and returns to low when R is high or S is low.

Rajah 2 (c)

[8 markah]

CLO1
C4

(d) Based on Figure 2 (d):

- (i) Identify the truth table for JK flip-flop with preset and clear inputs.
- (ii) Draw the output for the flip-flop. Given $Q_{\text{initial}}=1$, Preset = Clear = 1, and clock is negative edge triggered.

Berdasarkan Rajah 2 (d):

- (i) *Kenalpasti jadual kebenaran bagi flip-flop JK dengan masukan preset dan clear.*
- (ii) *Lukiskan keluaran bagi flip-flop. Diberi $Q_{\text{awal}}=1$, Preset = Clear = 1 dan picuan pinggir negatif.*

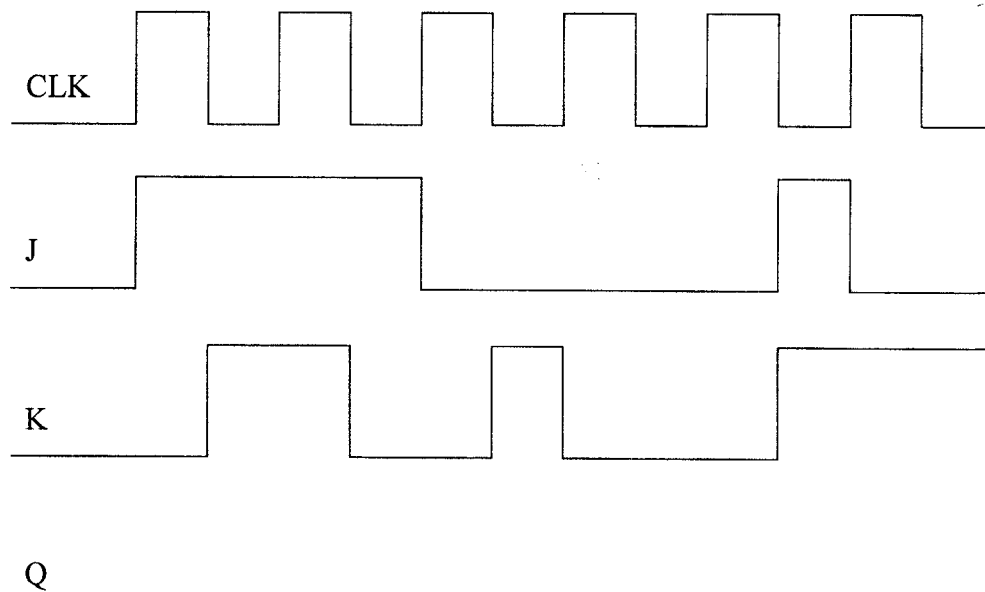


Figure 2(d)

Rajah 2(d)

[6 marks]

[6 markah]

QUESTION 3
SOALAN 3

CLO1
C2

- (a) An asynchronous counter (up counter) has 2MHz input frequency. The output frequency for the last flip-flop is 125 kHz. Determine:
- The numbers of flip-flops required.
 - The frequency input for the third flip-flop.
 - The logic circuit.

Pembilang tak bergerak (bilang ke atas) mempunyai frekuensi masukan 2MHz.

Frekuensi keluaran flip-flop yang terakhir 125 kHz. Tentukan:

- Bilangan flip-flop yang diperlukan.*
- Frekuensi masukan flip-flop ketiga.*
- Litar logic.*

[9 marks]
[9 markah]

CLO1
C3

- (b) Refer to Figure 3 (b), sketch a synchronous counter using JK flip-flop by following the sequence number. Illustrate:
- Excitation table.
 - Karnaugh map and Boolean expression.
 - The logic circuit.

Merujuk Rajah 3 (b), lakarkan pembilang bergerak menggunakan flip-flop JK mengikut turutan nombor. Gambarkan:

- Jadual Ujaan.*
- Peta Karnaugh dan ungkapan Boolean.*
- Litar logic.*

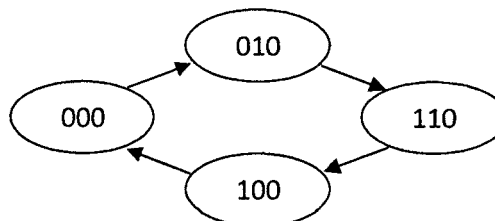


Figure 3 (b)

Rajah 3 (b)

[10 marks]
[10 markah]

CLO1
C4

- (c) Draw the circuit of the asynchronous counter MOD 8 using JK flip-flop negative trigger. Determine:

Lukiskan litar pembilang tak segera MOD 8 menggunakan flip-flop JK picuan negatif. Tentukan:

[2 marks]

[2 markah]

- (i) The number of flip-flop.

Bilangan flip-flop yang diperlukan.

[1 mark]

[1 markah]

- (ii) The maximum decimal number

Nombor desimal maksimum.

[1 mark]

[1 markah]

- (iii) The state diagram.

Rajah keadaan.

[2 marks]

[2 markah]

QUESTION 4
SOALAN 4CLO1
C2

- (a) Identify **TWO (2)** methods of shift register by using diagrams. (Use input data "10010" as reference)

*Dengan bantuan gambarajah, kenalpasti **DUA (2)** kaedah menganjak data (Gunakan data masukan "10010" sebagai rujukan).*

[6 marks]

[6 markah]

CLO1
C3

- (b) If series data "1010110" is shifted to 5-bit shift register series input / series output (SISO):

Jika data siri "1010110" dianjak ke dalam daftar anjakan 5 bit masukan siri / keluaran siri (SISO):

- i. Sketch the timing diagram that shows the shifted data.

Lakarkan rajah masa bagi menunjukkan anjakan data.

[5 marks]

[5 markah]

- ii. Calculate the required time for 5-bit data above if the clock pulse frequency is 500 Hz and 8 MHz.

Kirakan masa yang diperlukan bagi menganjak data 5 bit di atas jika frekuensi denyut jam ialah 500Hz dan 8MHz.

[3 marks]

[3 markah]

CLO1
C3

- (c) Refer to Figure 4(c) below, given $R_1 = 150\text{ k}\Omega$, $R_2 = 75\text{ k}\Omega$, $R_3 = 37.5\text{ k}\Omega$, $R_4 = 18.7\text{ k}\Omega$ and $R_f = 20\text{ k}\Omega$. Calculate the value of the output, V_{out} for a digital entries below:

- Binary input = 0010
- Binary input = 0101

Merujuk pada Rajah 4(c) di bawah, diberi $R_1 = 150\text{ k}\Omega$, $R_2 = 75\text{ k}\Omega$, $R_3 = 37.5\text{ k}\Omega$, $R_4 = 18.7\text{ k}\Omega$ dan $R_f = 20\text{ k}\Omega$. Kirakan nilai voltan keluaran V_{out} untuk masukan digital di bawah:

- Masukan Binari = 0010
- Masukan Binari = 0101

[11 marks]

[11 markah]

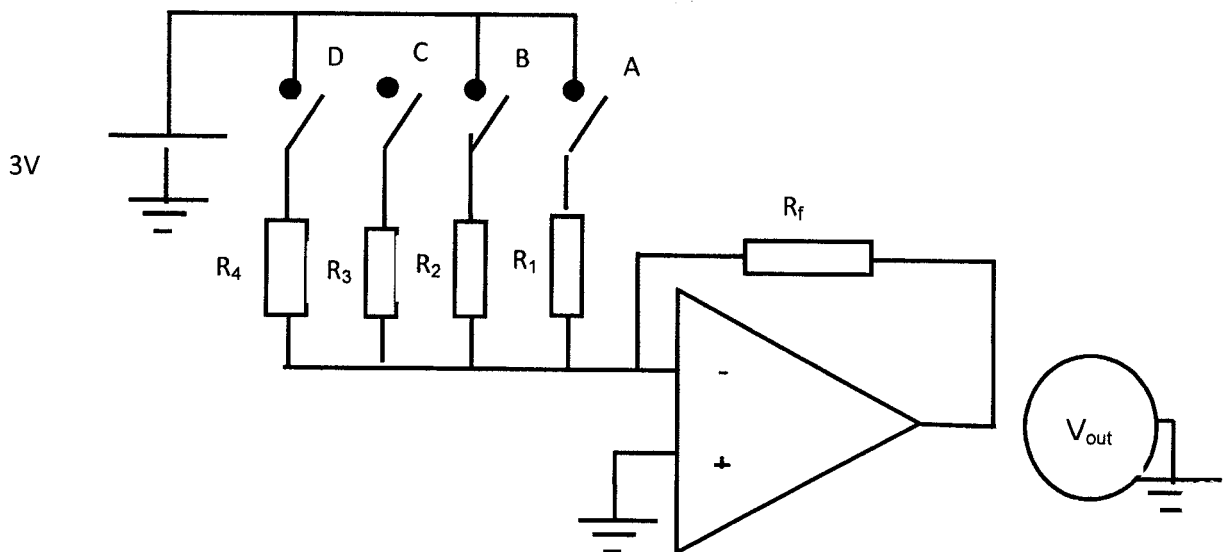


Figure 4 (c)

Rajah 4 (c)

SOALAN TAMAT