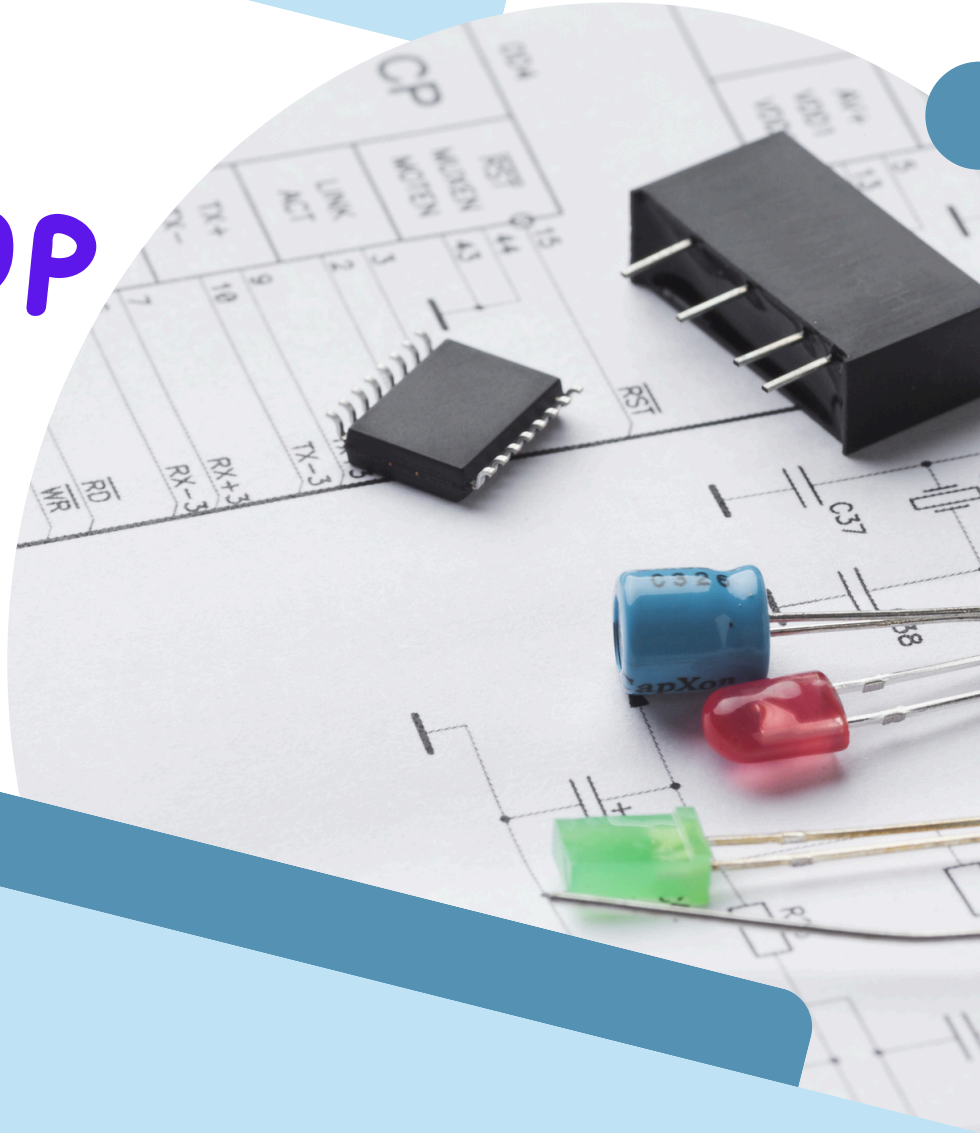
DIGITAL ELECTRONICS

VOLUME 2

FLIP FLOP



NORAZITA BINTI IBRAHIM
PUTERI NADIA DAYANIE BINTI MEGAT SABRI

FLIP-FLOP

DIGITAL ELECTRONICS

VOLUME 2

By:
NORAZITA BINTI IBRAHIM
PUTERI NADIA DAYANIE BINTI MEGAT SABRI

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ACKNOWLEDGEMENTS

Bismillahirrahmanirrohim
In the name of Allah, the Most Gracious and the Most Merciful.

Alhamdulillah, first and foremost, we want to praises and thanks to Allah for completing our second e-book successfully. Without his will we would not be able to complete this e-book.

Secondly, special thanks to Polytechnic Ungku Omar especially Electrical Engineering Department, for providing us with the inspiration and opportunity to create this e-book.

We would like to extend my deepest gratitude to our family for their unwavering support and encouragement throughout this journey.

We hope that this e-book will be beneficial, especially to students, and provide valuable insights and knowledge that can aid in their studies.

Thank you all for your support and contributions, which have made this e-book possible.

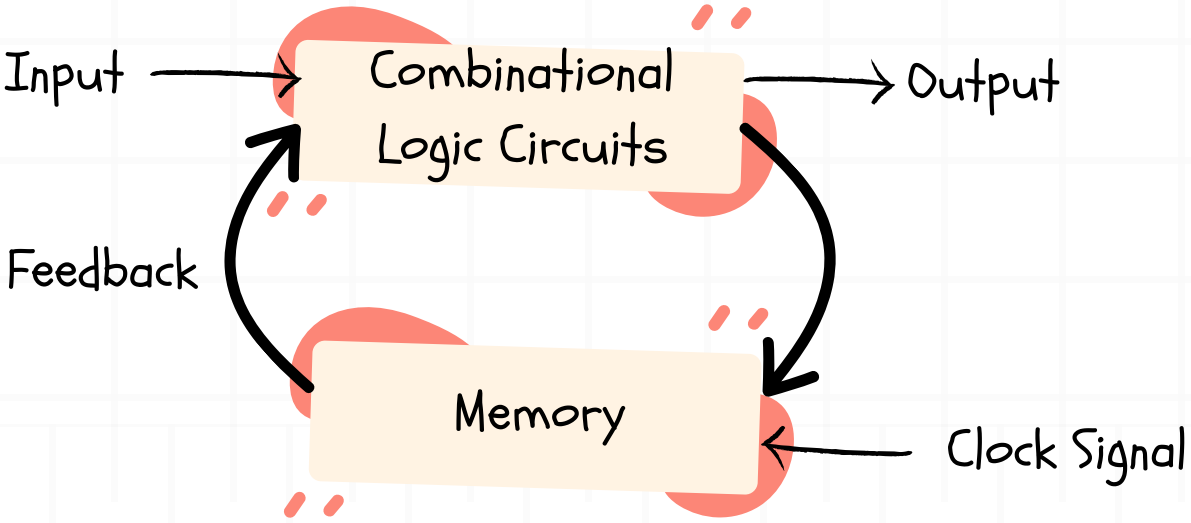
PREFACE

This book, Digital Electronics Volume 2, focuses on Chapter 3, which covers Flip-Flops. The chapter introduces the fundamental concepts of Flip-Flops, offering a clear understanding of their circuits, truth tables, and timing diagrams. Designed to aid students in mastering these essential topics, this e-book includes concise explanations, practical examples, and exercises for each subtopic. These resources are intended to reinforce learning and deepen comprehension of Flip-Flop circuits and their applications.

CONTENTS

3.0 FLIP-FLOP

INTRODUCTION



Combinational Logic Circuits

- No memory
- Change state depending upon the actual signals being applied to their inputs

Sequential Logic Circuits

- Have some form of inherent "Memory"
- Each of inputs and outputs can either of 2 stages:
  - Logic 0
  - Logic 1

3.1 REMEMBER TYPES OF FLIP-FLOPS

What is flip-flop?

Flip-flop is a kind of bistable multivibrator.
It is a Sequential Circuit which has two stable states and is capable of serving as one bit of memory, bit 1 or bit 0.

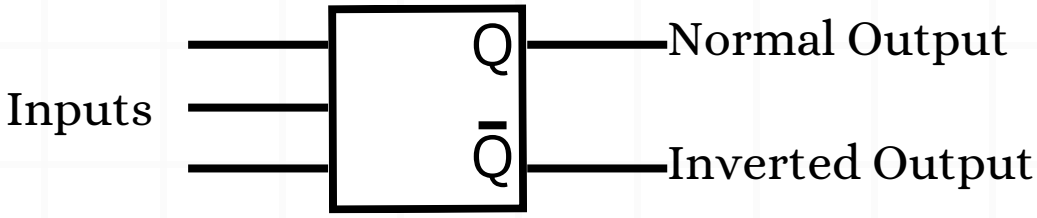
Flipped

- High/Set
- Logic ‘1’
  $Q=1, \bar{Q}=0$

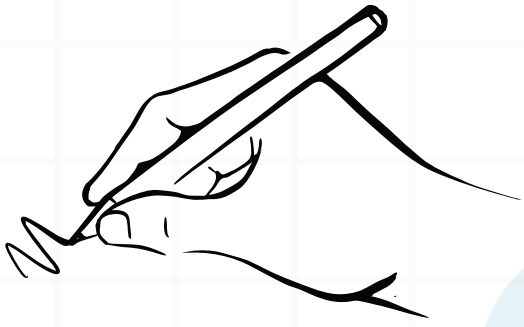
Flopped

- Low/Reset
- Logic ‘0’
  $Q=0, \bar{Q}=1$

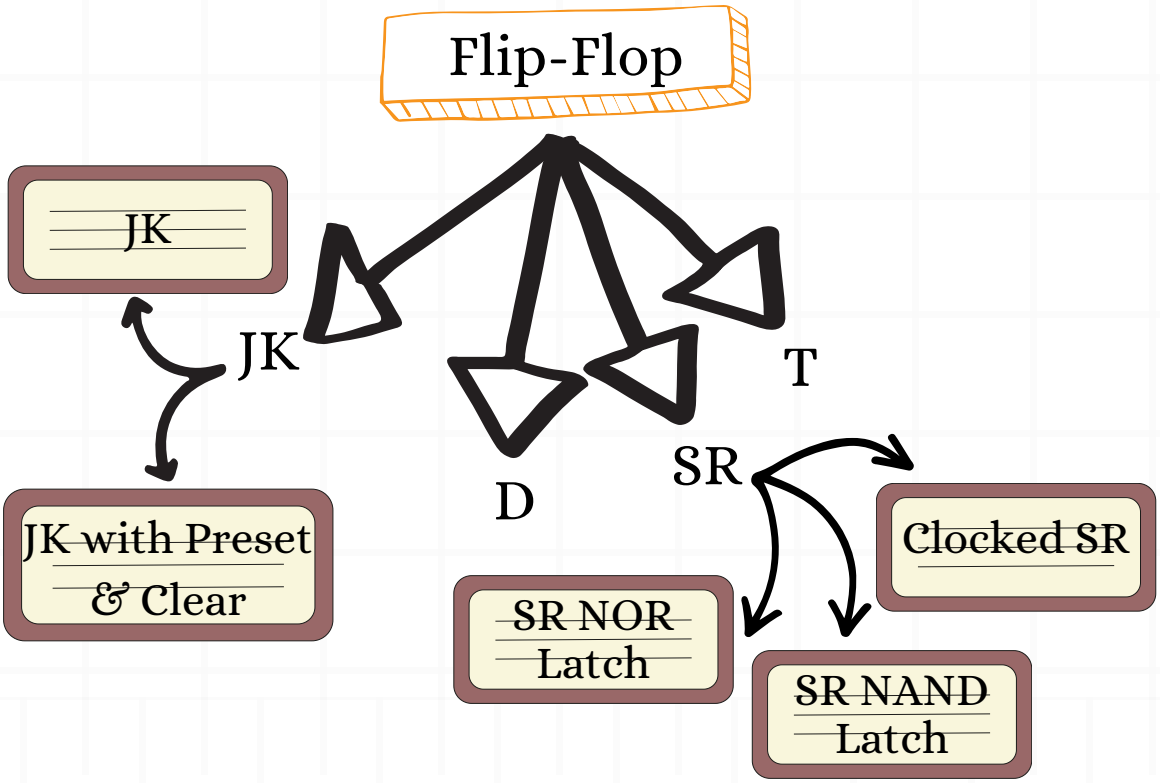
General Flip-Flop symbol



- Have two stable conditions.
- Can be switched from one to the other by appropriate inputs.
- Stable conditions usually called the **states**. (1=High, 0=Low)
- Q is normal output.
- More complicated Flip-Flop use a clock as the control input.



Types of Flip-Flop



Used of Flip-Flop

- For memory circuits
- For logic control devices
- For counter devices
- For register devices

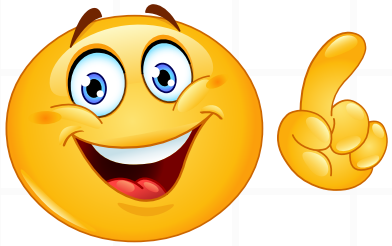
3.2 UNDERSTAND OPERATION OF EACH TYPE OF FLIP-FLOP

SR Flip-Flop

- Basic flip-flop and is an asynchronous counter.
- The outputs is immediately change anytime one or more of the inputs change just as in combinational logic circuit.
- Does not operate in step with a clock or timing.
- Can be constructed using two NAND gates latch or two NOR gates latch.

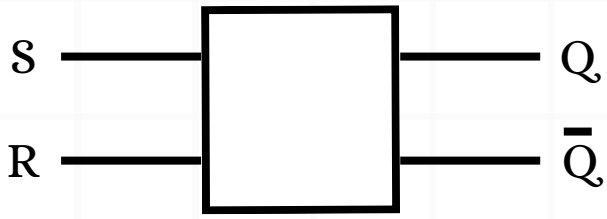
Latch

- Active low = NAND gates
- Active high = NOR gates



SR Flip-Flop

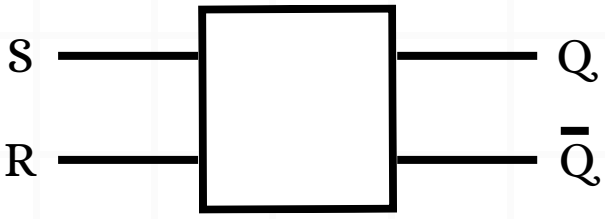
Logic symbol



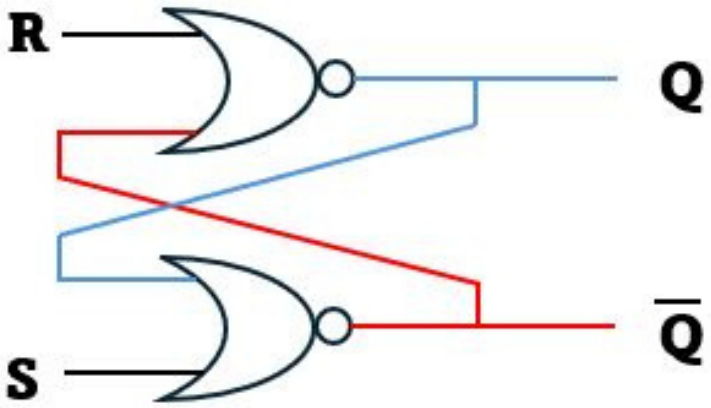
- Has two inputs, SET (S) and RESET (R).
- Has two outputs, Q and $\overline{Q}$.
- Q is the normal output and is the one most used.
- $\overline{Q}$ is simply the compliment of output Q.

SR NOR Latch

Logic symbol / Block Diagram



Logic Circuit

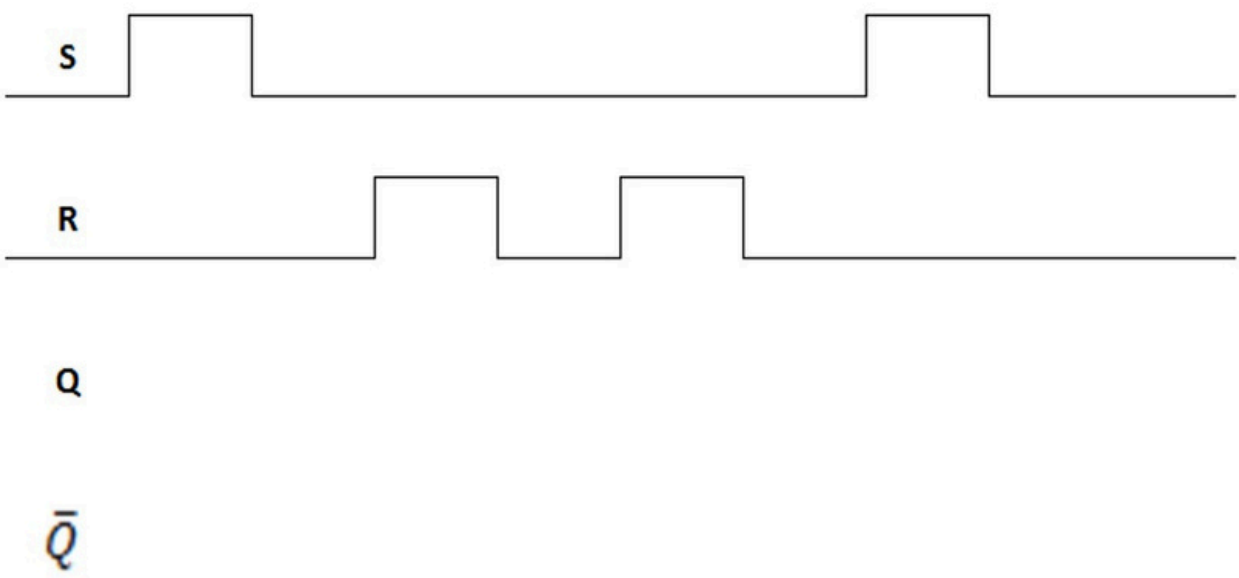


SR NOR Latch

Truth Table

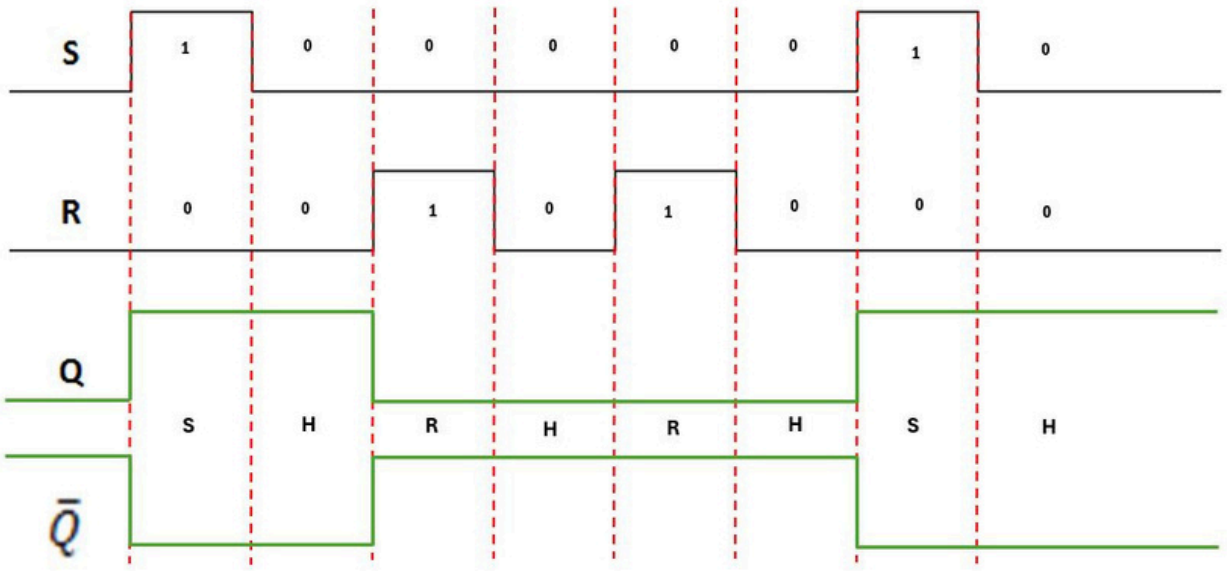
INPUT		OUTPUT		MODE OF OPERATION
S	R	Q	$\bar{Q}$	
0	0	Q	$\bar{Q}$	HOLD (H)
0	1	0	1	RESET (R)
1	0	1	0	SET (S)
1	1	0	0	INVALID (INV)

Example 1: Draw the output Timing Diagram for SR NOR Latch, initial Q is 0.



SR NOR Latch

Answer 1

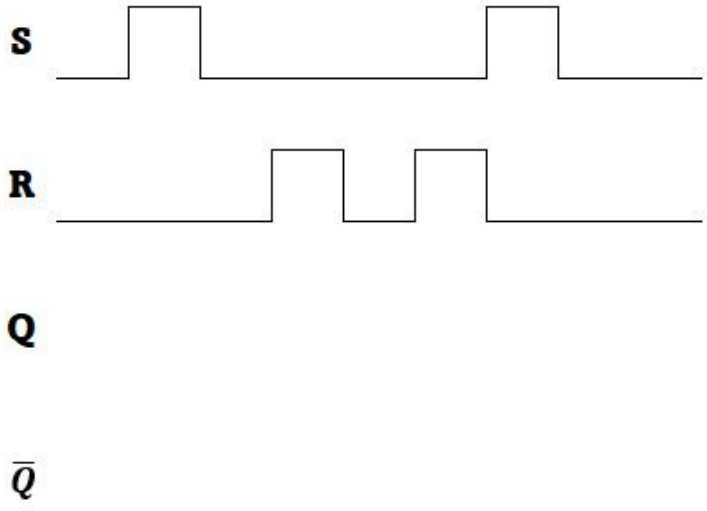


Try this!

1.Complete the truth table for SR NOR Latch below.

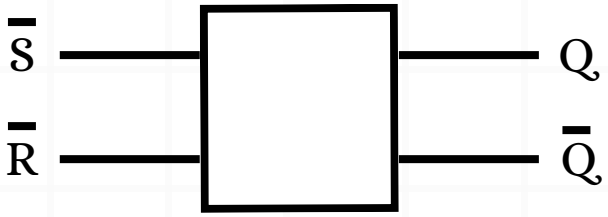
Input		Output		Mode of Operation
S	R	Q	$\bar{Q}$	
1	0			
0	0			
0	1			
0	0			
1	1			
1	0			
0	1			
0	0			

2.Draw the output Timing Diagram for SR NOR Latch, initial Q is 0.

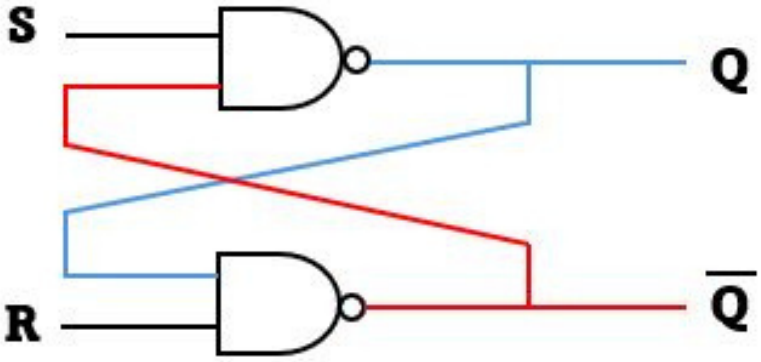


SR NAND Latch

Logic symbol / Block Diagram



Logic Circuit

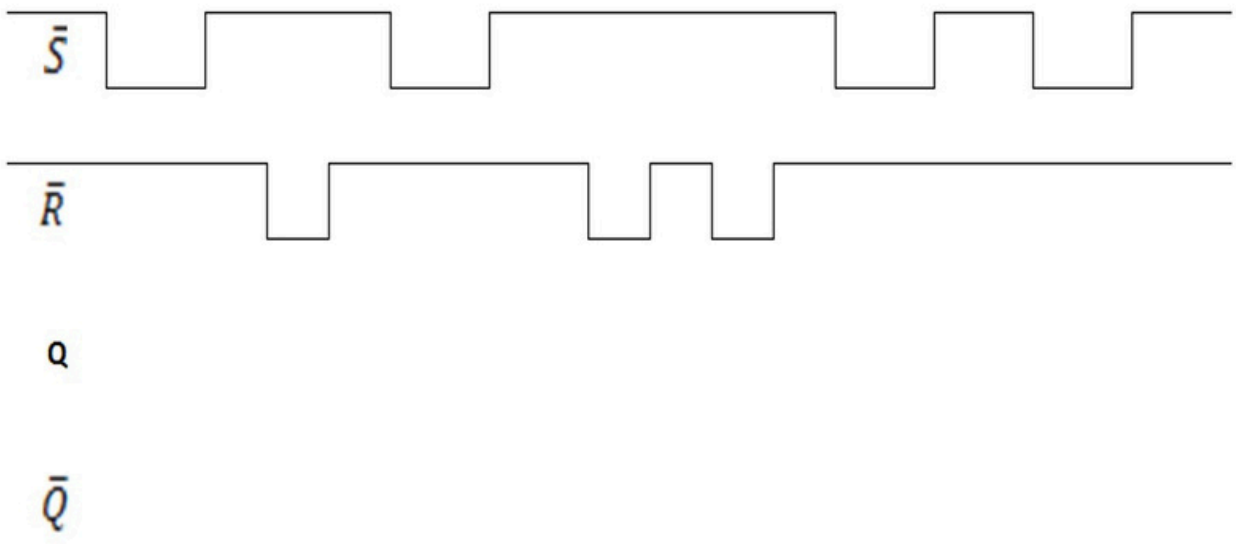


SR NAND Latch

Truth Table

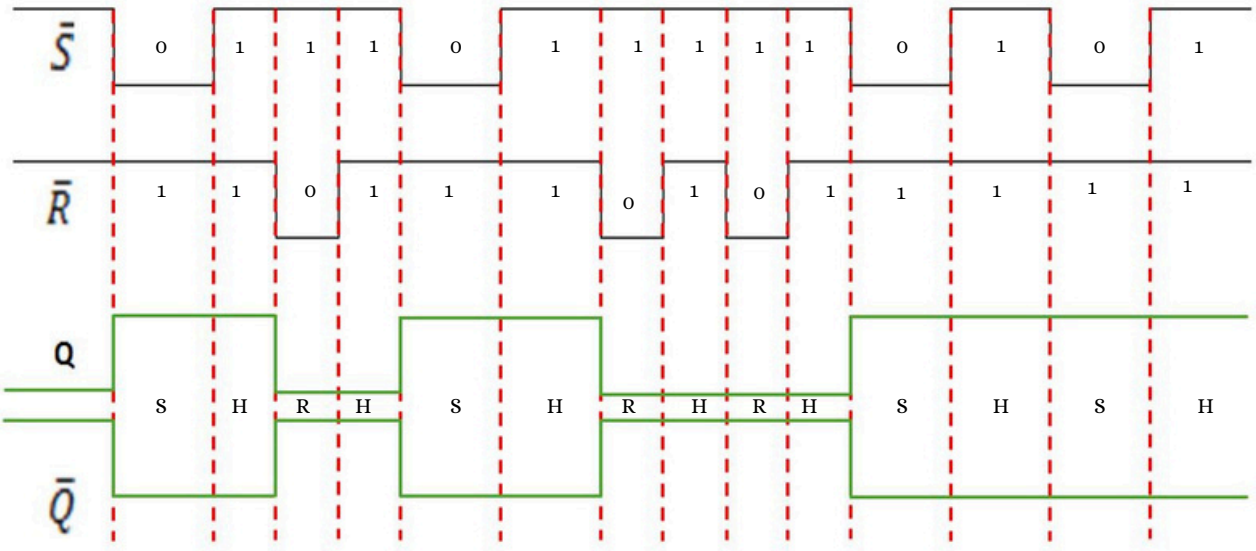
INPUT		OUTPUT		MODE OF OPERATION
S	R	Q	$\bar{Q}$	
0	0	1	1	INVALID (INV)
0	1	1	0	SET (S)
1	0	0	1	RESET (R)
1	1	Q	$\bar{Q}$	HOLD (H)

Example 2: Draw the output Timing Diagram for SR NAND Latch, initial Q is RESET.



SR NAND Latch

Answer 2:

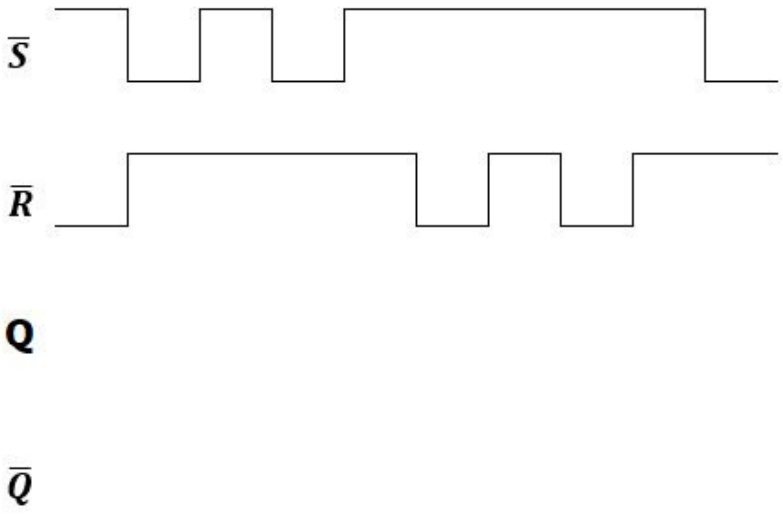


Try this!

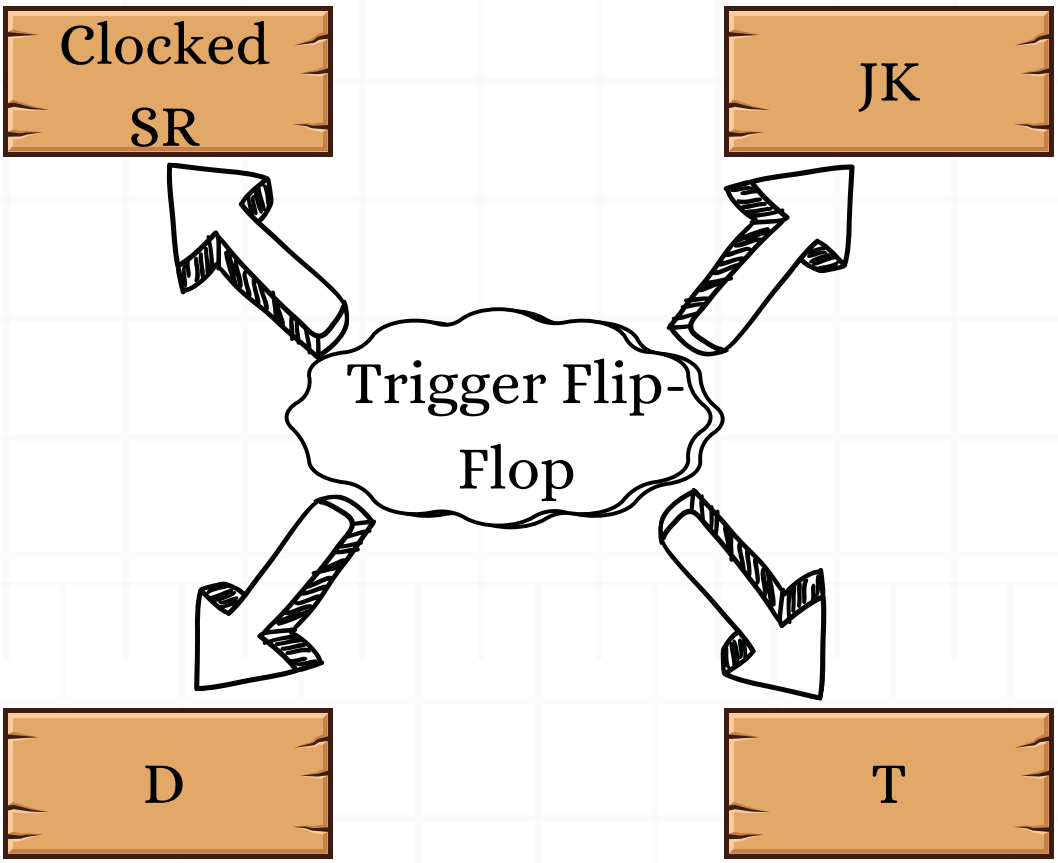
1.Complete the truth table for SR NAND Latch below.

Input		Output		Mode of Operation
S	R	Q	$\bar{Q}$	
0	1			
1	0			
0	1			
1	1			
0	0			
1	0			
0	1			
1	1			

2.Draw the output Timing Diagram for SR NOR Latch, initial Q is 0.



Trigger Flip-Flop (Sequential Circuits)



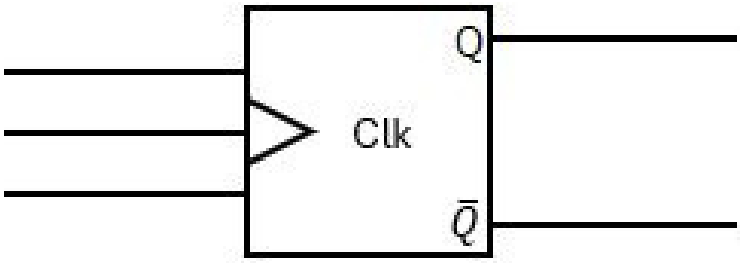
- Depends on clock pulse applied to their inputs.
- The result of flip-flop responding to a clock input is called clock-pulse-triggering.
- 2 types: a) Positive Edge Triggering (PGT)
  b) Negative Edge Triggering (NGT)

The Clock

- The exact times at which any output can change states are controlled by a signal.
- Clock signal is generally a rectangular pulse train or a square wave.
- Clock is distributed to all parts of the system, and most of the system outputs can change state only when the clock makes a transition.
- PGT - clock changes from a LOW state to a HIGH state.
- NGT - clock changes from a HIGH state to a LOW state.

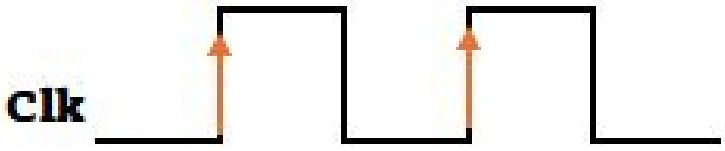
Positive Edge Triggering (PGT)

Block Diagram



Positive Edge Triggering (PGT)

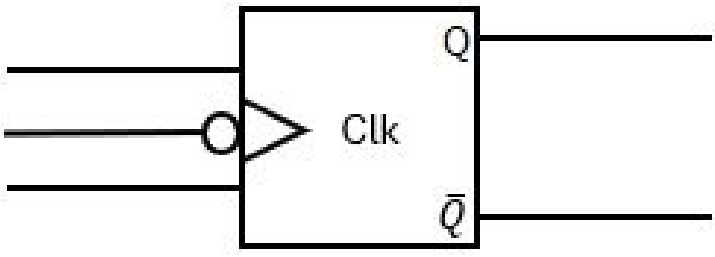
Timing Diagram



- Triggering on the edge of the clock pulse.
- Low to High transition of clock pulse.

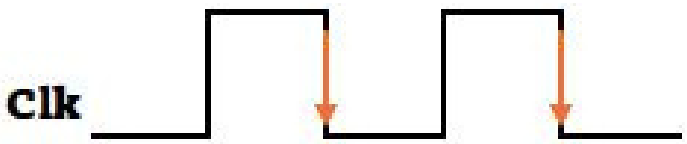
Negative Edge Triggering (NGT)

Block Diagram



Negative Edge Triggering (NGT)

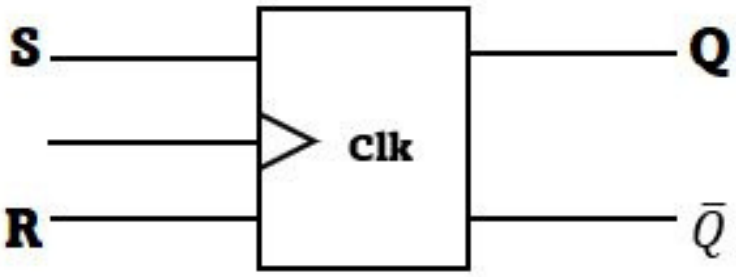
Timing Diagram



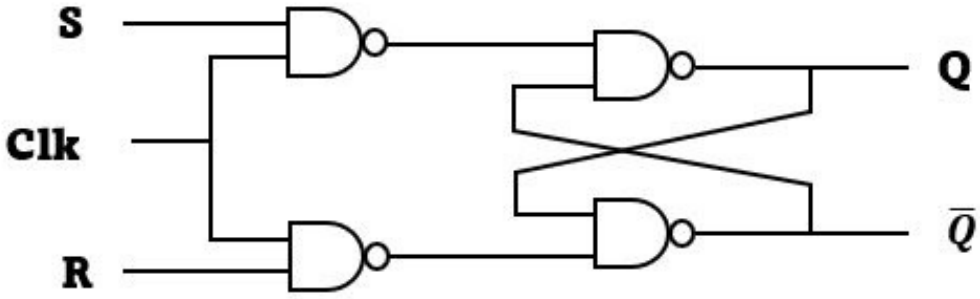
- Triggering on the edge of the clock pulse.
- High to Low transition of clock pulse.

CLOCKED SR FLIP-FLOP

Logic symbol / Block Diagram



Logic Circuit



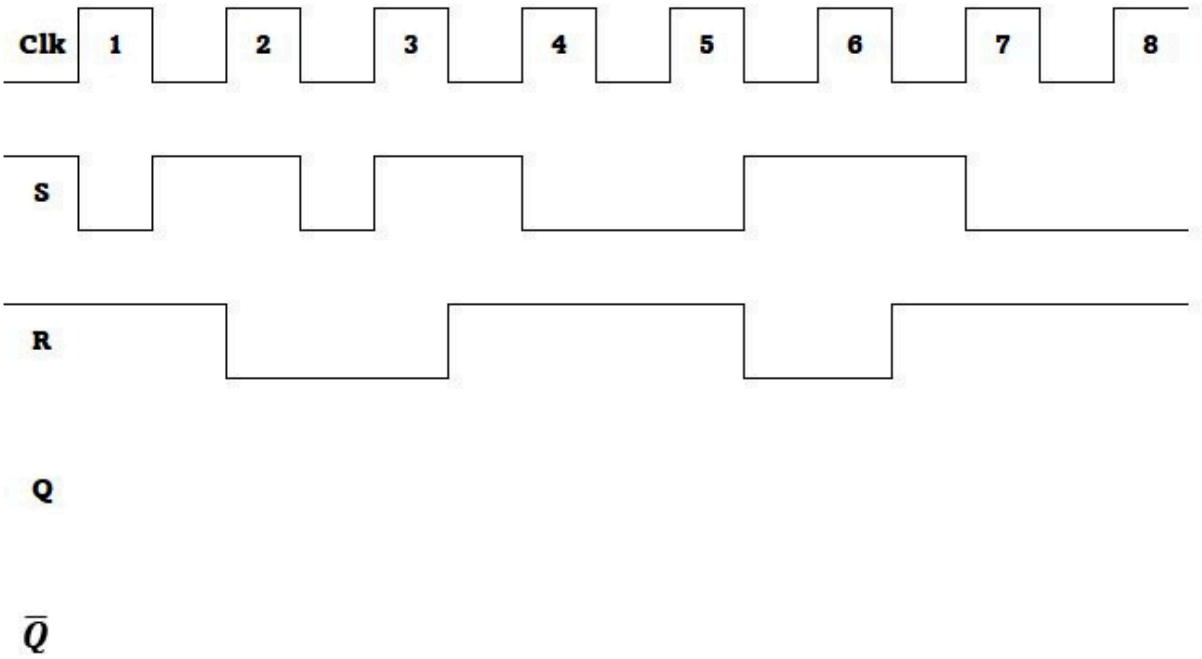
CLOCKED SR FLIP-FLOP

Truth Table

INPUT			OUTPUT		MODE OF OPERATION
CLK	S	R	Q	$\overline{Q}$	
1	0	0	Q	$\overline{Q}$	HOLD (H)
1	0	1	0	1	RESET (R)
1	1	0	1	0	SET (S)
1	1	1	1	1	INVALID (INV)
0	X	X	Q	$\overline{Q}$	HOLD (H)

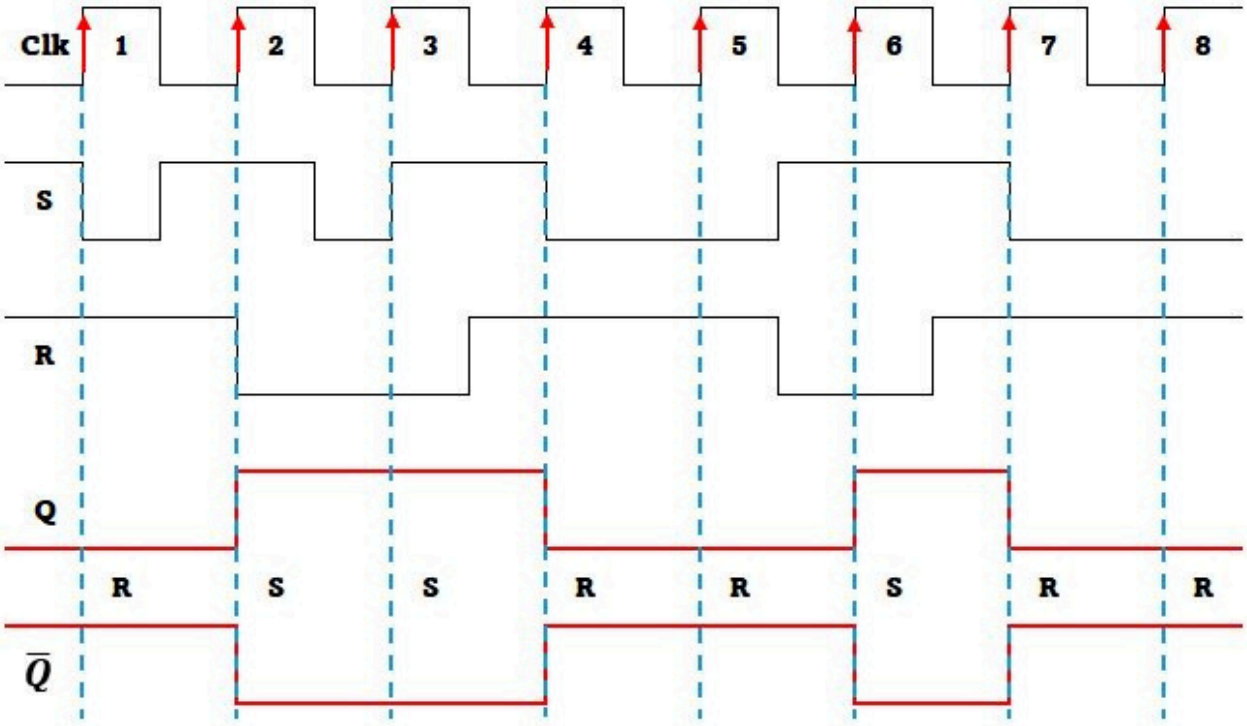
Example 3

Draw the output Q and $\overline{Q}$ waveform for positive edge trigger Clocked SR flip-flop. Initial Q is RESET.



CLOCKED SR FLIP-FLOP

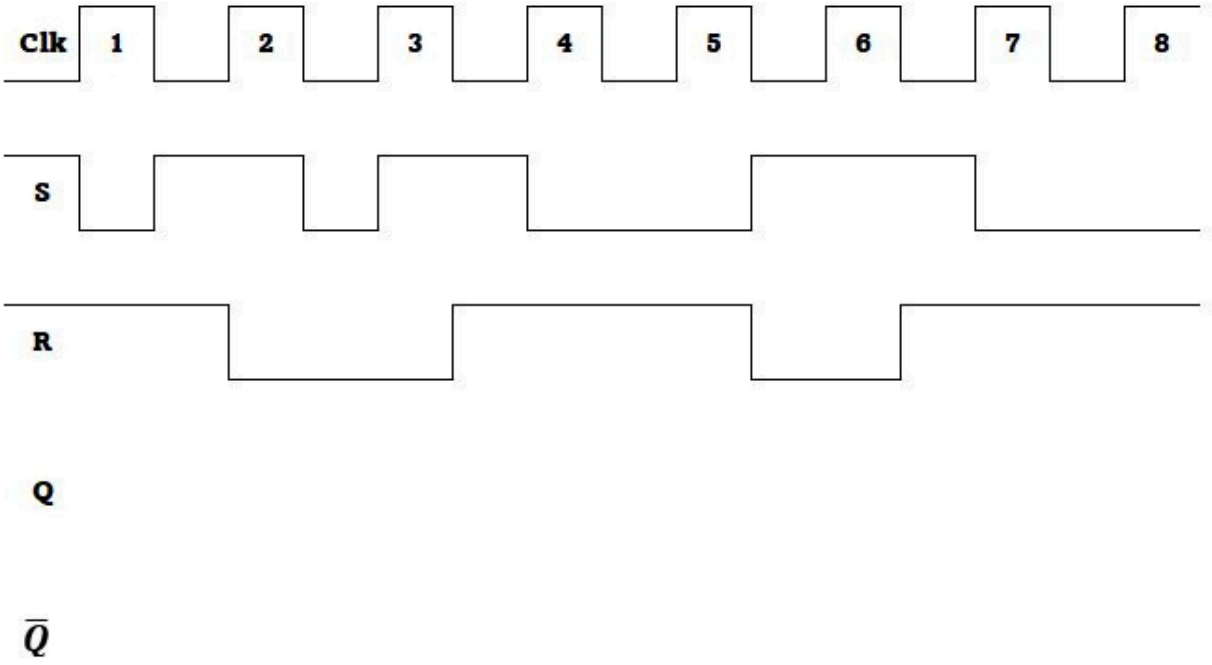
Answer 3



CLOCKED SR FLIP-FLOP

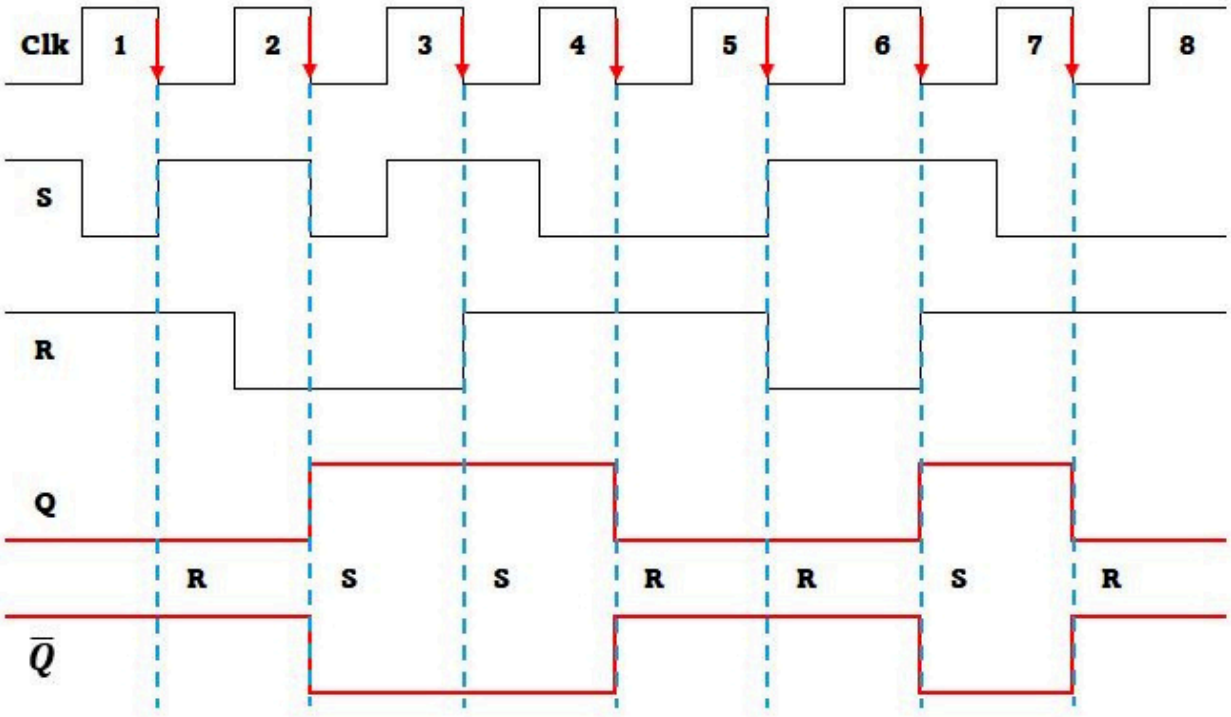
Example 4

Draw the output Q and $\overline{Q}$ waveform for negative edge trigger Clocked SR flip-flop. Initial Q is RESET.



CLOCKED SR FLIP-FLOP

Answer 4

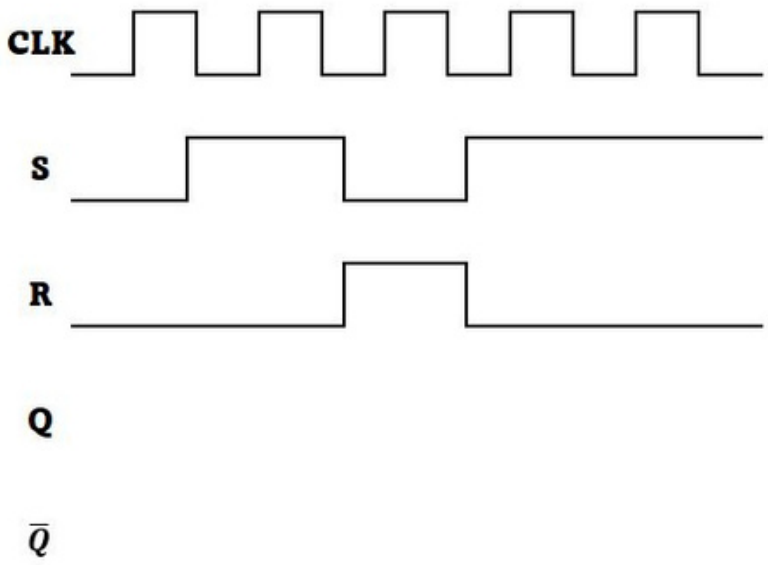


Try this!

1.Complete the truth table for CLOCKED SR flip-flop below.

Input			Output		Mode of Operation
Clock	S	R	Q	$\bar{Q}$	
1	1	0			
0	0	1			
1	0	1			
1	0	0			
0	1	1			
1	1	1			
1	1	0			
0	0	1			

2.Draw the output Q and $\overline{Q}$ waveform for positive edge trigger Clocked SR flip-flop. Initial Q is RESET.



QUIZ TIME

INSTRUCTION:
Answer all question in 15 minutes

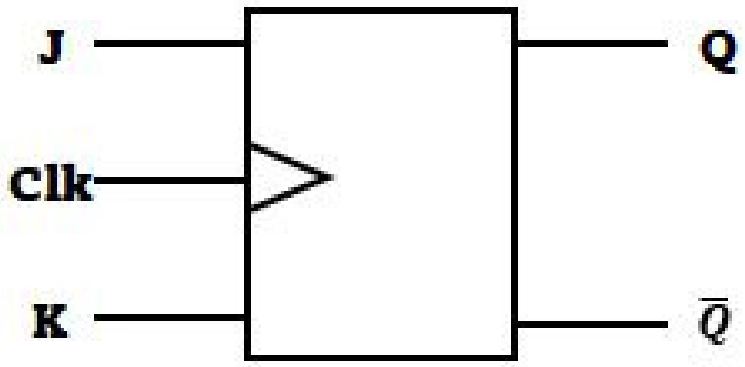
Scan me!

Submit your answer here

JK FLIP-FLOP

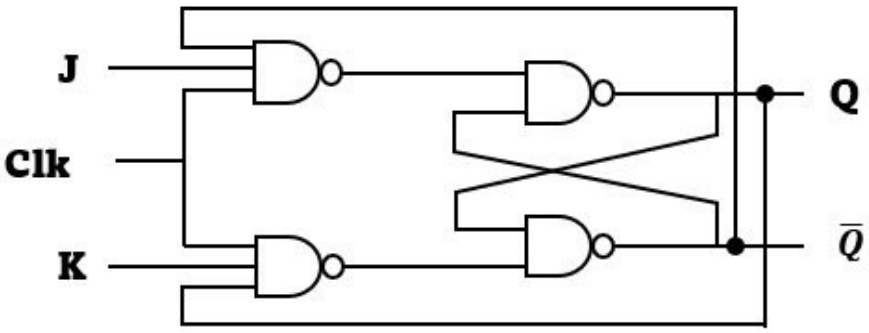
- Versatile and widely used type of flip-flop.
- Functioning of JK is same of the SR in the SET, RESET and HOLD conditions of operation.
- The difference is, the JK flip-flop has no INVALID state as does the SR flip-flop.
- When J and K inputs are HIGH (1), output is TOGGLE (change condition) mode.
- JK flip-flop connected for TOGGLE operation is sometimes called a T flip-flop.

Logic symbol / Block Diagram



JK FLIP-FLOP

Logic Circuit

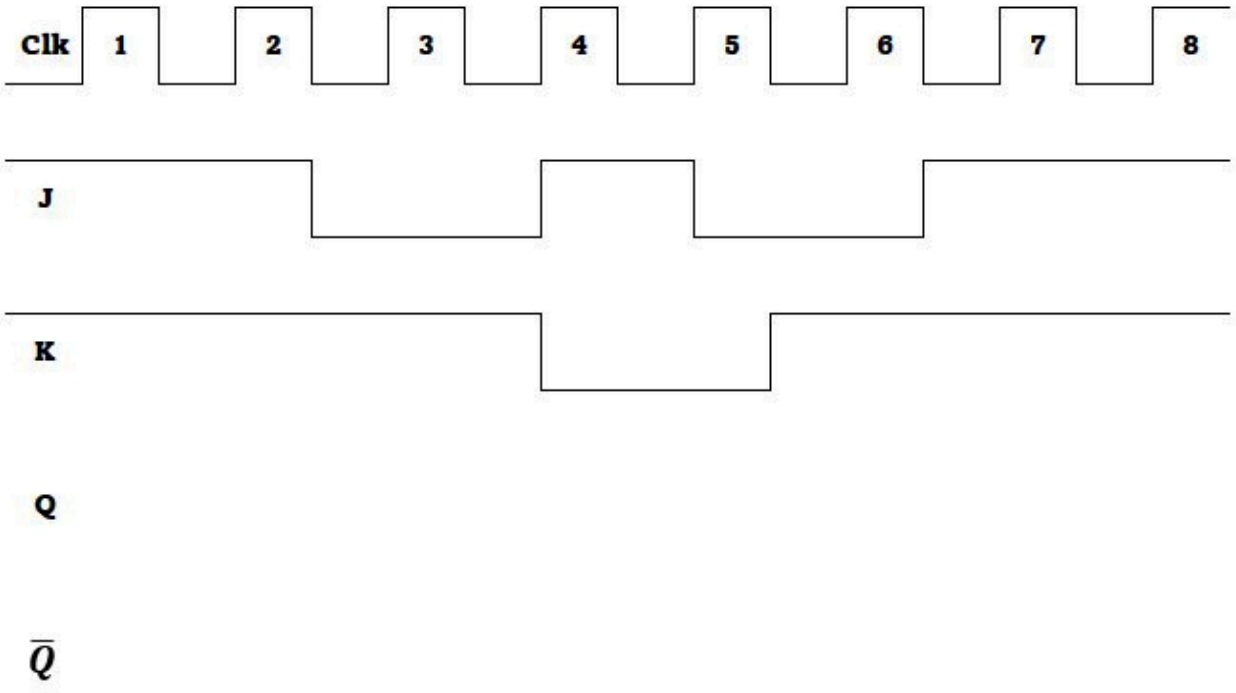


Truth Table

INPUT			OUTPUT		MODE OF OPERATION
CLK	J	K	Q	$\overline{Q}$	
1	0	0	Q	$\overline{Q}$	HOLD (H)
1	0	1	0	1	RESET (R)
1	1	0	1	0	SET (S)
1	1	1	$\overline{Q}$	Q	TOGGLE (T)
0	X	X	Q	$\overline{Q}$	HOLD (H)

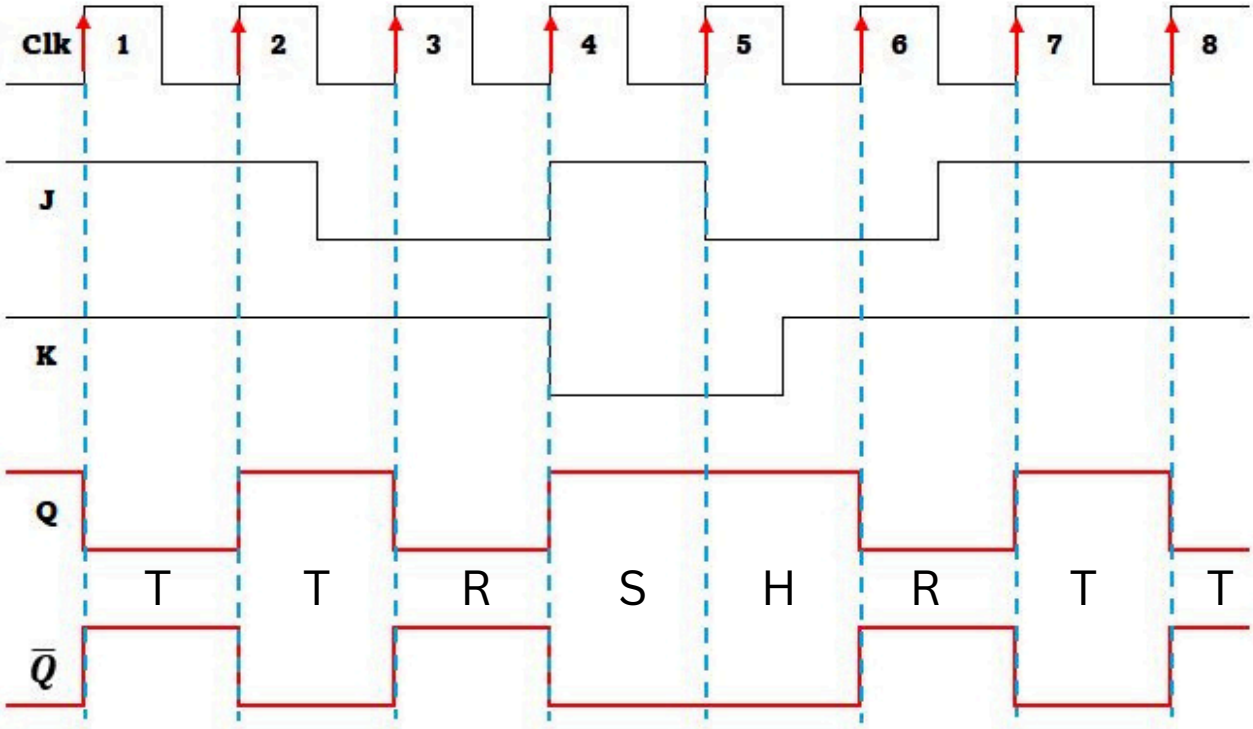
JK FLIP-FLOP

Example 5 Draw the output Q and $\overline{Q}$ waveform for positive edge trigger JK flip-flop. Initial Q is SET.



JK FLIP-FLOP

Answer 5

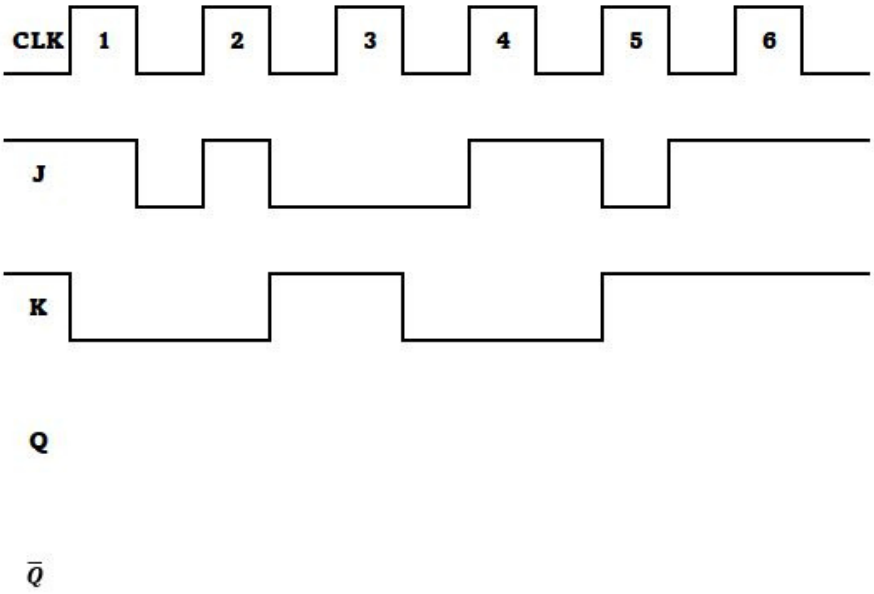


Try this!

1. Complete the table below for the output and mode of operation for JK flip-flop.

INPUT		BEFORE CLOCK		AFTER CLOCK		MODE OF OPERATION
J	K	Qn	$\overline{Qn}$	Qn+1	$\overline{Qn+1}$	
0	1	1	0			
1	0	0	1			SET
1	1			0	1	TOGGLE
0	0	0	1			
1	1	0	1			
0	1	1	0			

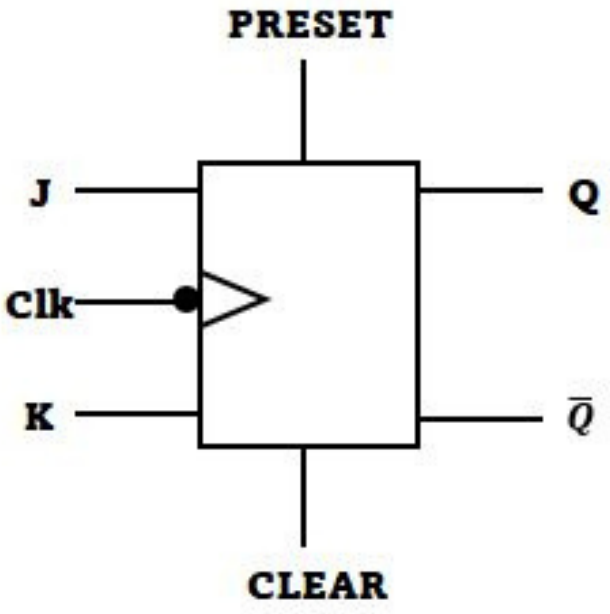
2. Based on figure below, sketch the output Q and $\overline{Q}$ for gated JK flip-flop with negative edge triggered. (Assume the initial Q=1)



JK FLIP-FLOP WITH PRESET AND CLEAR

- This flip-flop can also have other inputs called Preset (or SET) and Clear that can be used for setting the flip-flop to 1 or resetting it to 0 by applying the appropriate signal to the Preset and Clear inputs.
- These inputs can change the state of the flip-flop regardless of synchronous inputs or the clock.

Logic symbol / Block Diagram



JK FLIP-FLOP WITH PRESET AND CLEAR

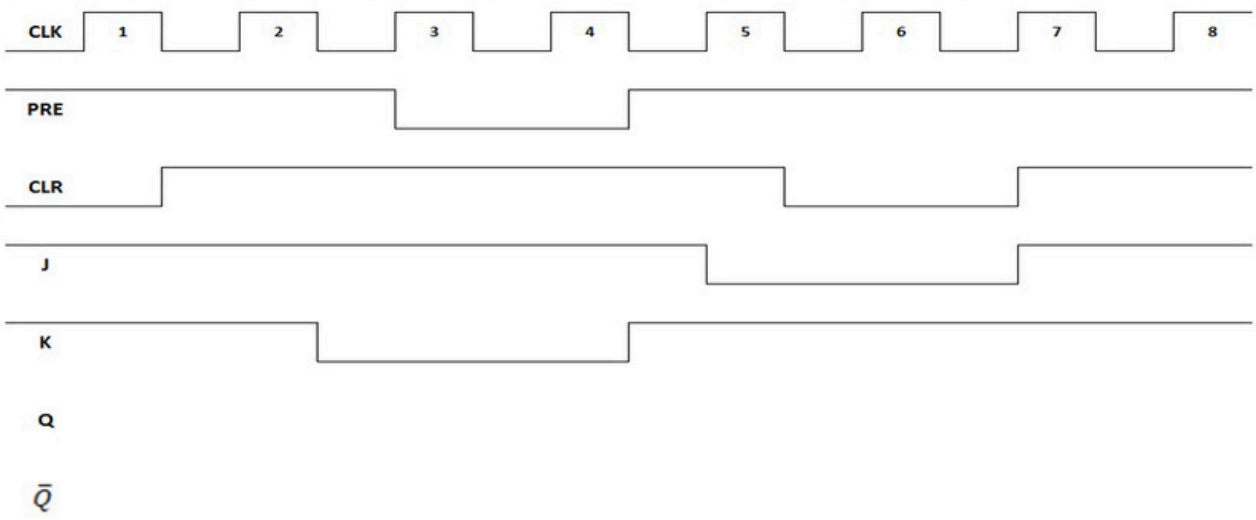
Truth Table

INPUT					OUTPUT		MODE OF OPERATION
Asynchronous		Synchronous			Q	$\overline{Q}$	
Preset	Clear	J	K	Clock			
0	0	X	X	X	1	1	INVALID (INV)
0	1	X	X	X	1	0	ASYNCHRONOUS SET
1	0	X	X	X	0	1	ASYNCHRONOUS RESET
1	1	0	0	1	Q	$\overline{Q}$	HOLD (H)
1	1	0	1	1	0	1	RESET (R)
1	1	1	0	1	1	0	SET (S)
1	1	1	1	1	$\overline{Q}$	Q	TOGGLE (T)

JK FLIP-FLOP WITH PRESET AND CLEAR

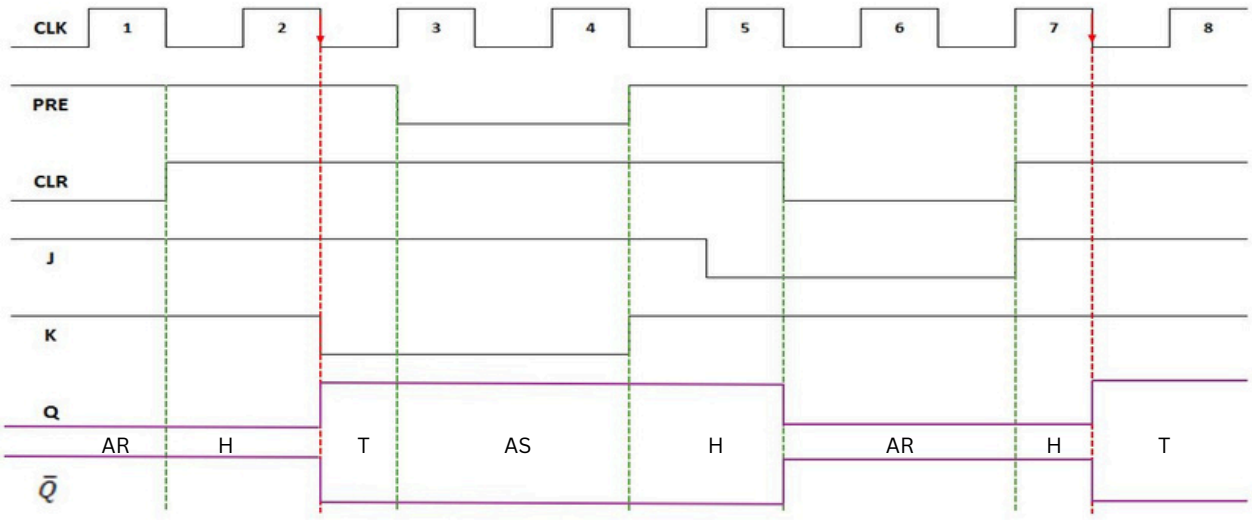
Example 6

Draw the output Q and $\overline{Q}$ waveform for negative edge trigger JK flip-flop with Preset and Clear. Initial Q is HIGH.



JK FLIP-FLOP WITH PRESET AND CLEAR

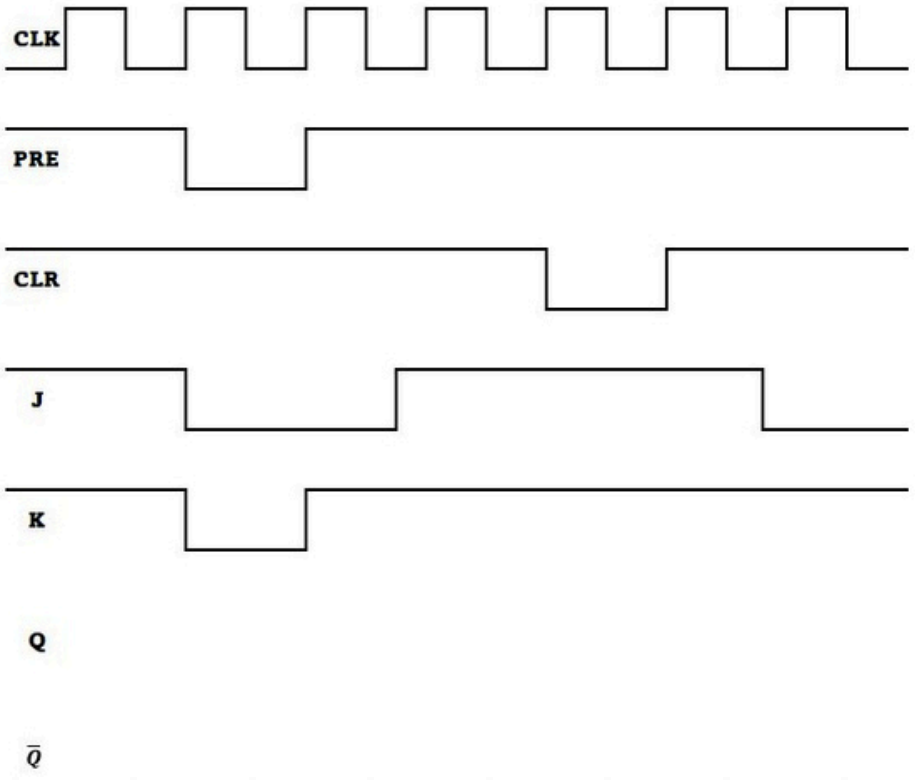
Answer 6



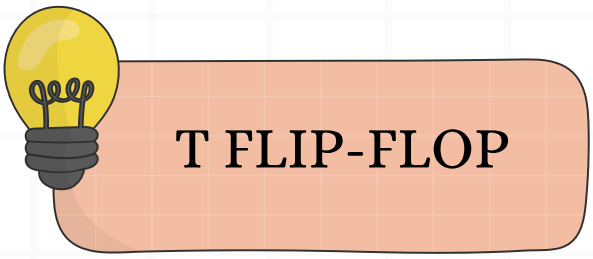
Try this!

1. By using a suitable diagram, explain the operation of the JK flip-flop with Preset (PR) and Clear (CLR).

2. The input for CLK, J, K, PRESET (PRE) and CLEAR (CLR) are shown in figure below. Express the output waveform for Q and $\overline{Q}$ if the flip-flop is a negative edge triggered and Q initial = 0.

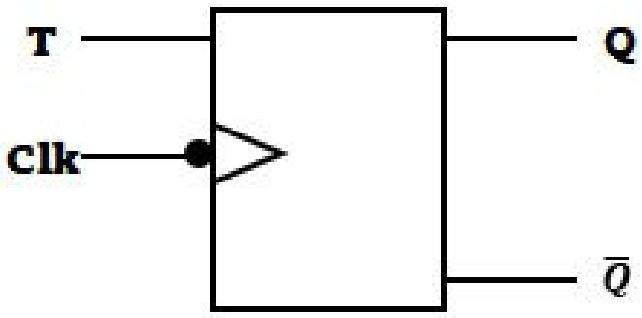


3.2 APPLY JK FLIP-FLOPS TO CONSTRUCT T FLIP-FLOP AND D FLIP-FLOP



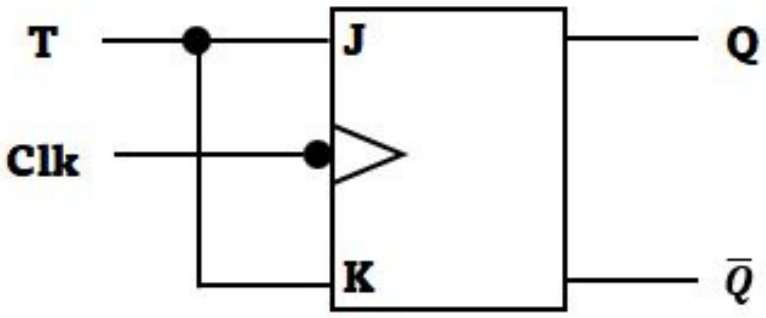
- Only have 1 input, T (Toggle), clock and output.
- Implementation from a JK flip-flop.

Symbol

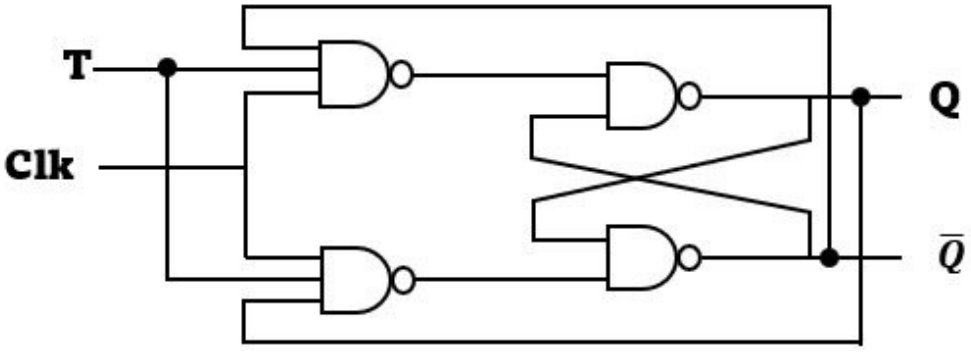


T FLIP-FLOP USING JK FLIP-FLOP

Block Diagram



Logic Circuit

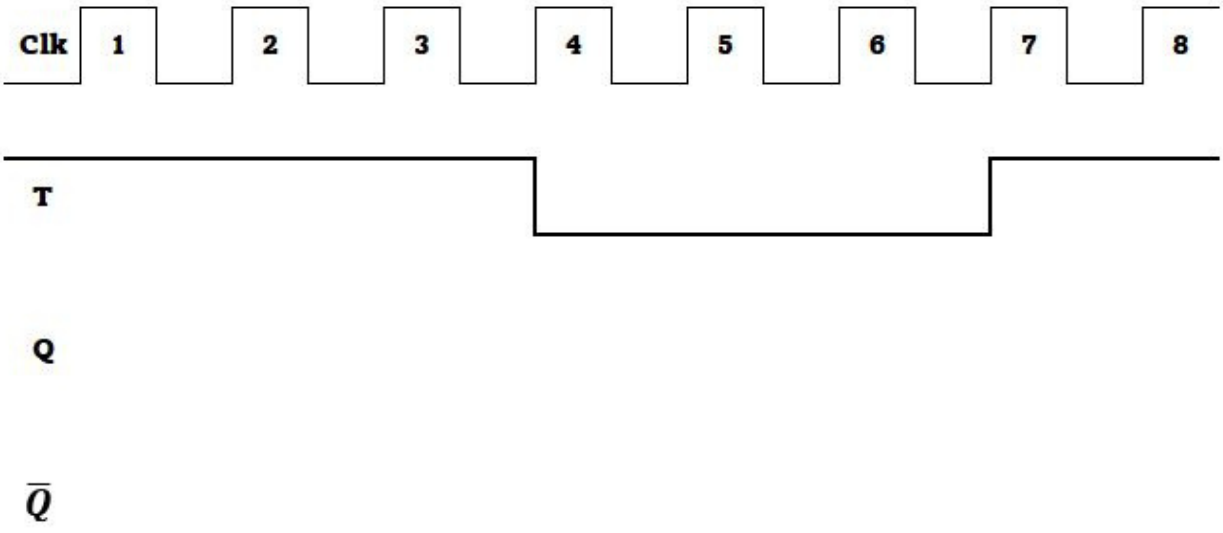


T FLIP-FLOP USING JK FLIP-FLOP

Truth Table

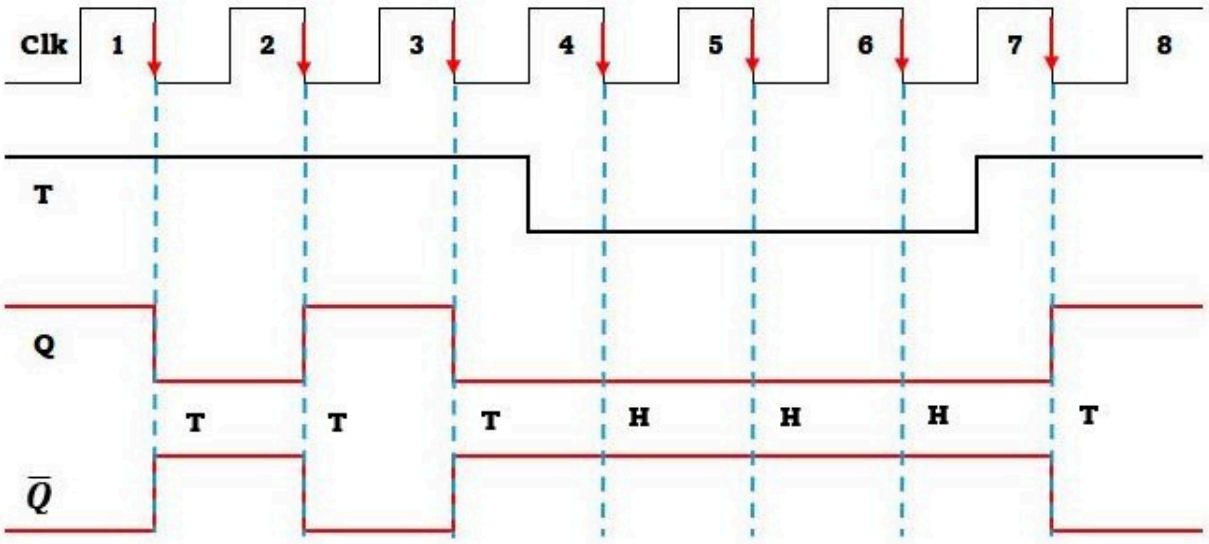
INPUT		OUTPUT		MODE OF OPERATION
CLK	T	Q	$\overline{Q}$	
1	0	Q	$\overline{Q}$	HOLD (H)
1	1	$\overline{Q}$	Q	TOGGLE (T)
0	X	Q	$\overline{Q}$	HOLD (H)

Example 7 Draw the output Q and $\overline{Q}$ waveform for negative edge trigger T flip-flop. Initial Q is SET.



T FLIP-FLOP USING JK FLIP-FLOP

Answer 7



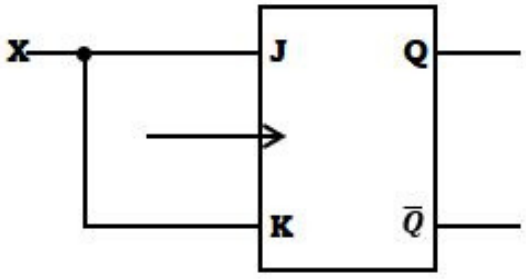
Try this!

1. State the output for T flip-flop as given in table below.

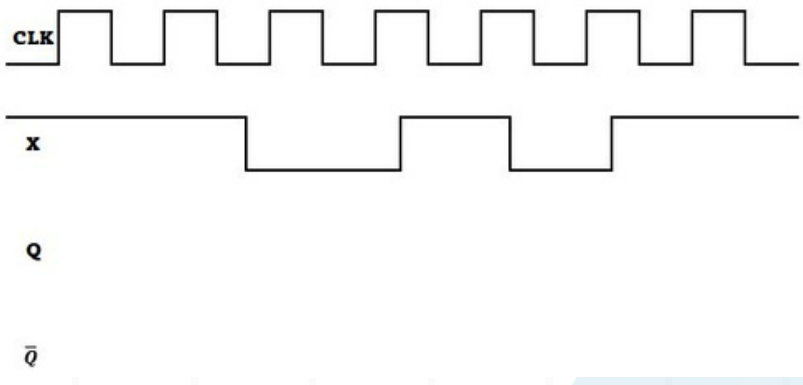
Input	Before Clock		After Clock	
T	Qn	$\overline{Qn}$	Qn+1	$\overline{Qn+1}$
1	1	0		
0	0	1	0	1
1	0		1	0
1	1	0		
0		1	0	1
1	0	1		

2. With the aid of diagram and truth table, explain how T flip-flop can be built by using JK flip-flop.

3(a). Identify the type and built the truth table of flip-flop shown in figure below.



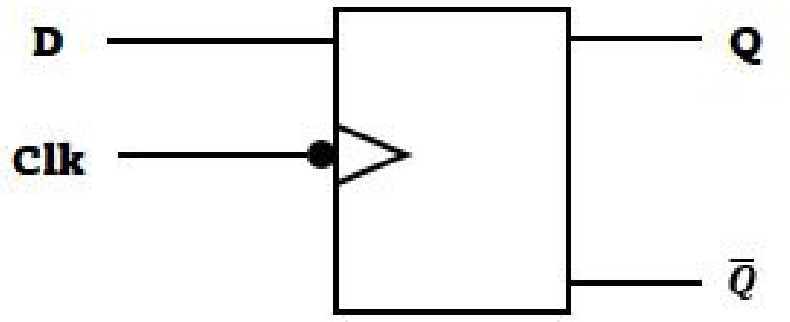
3(b). Sketch the output Q and $\overline{Q}$ for the flip-flop in 3(a) if the input X is given in figure below. Initial Q is 0 and clock is negative.



D FLIP-FLOP

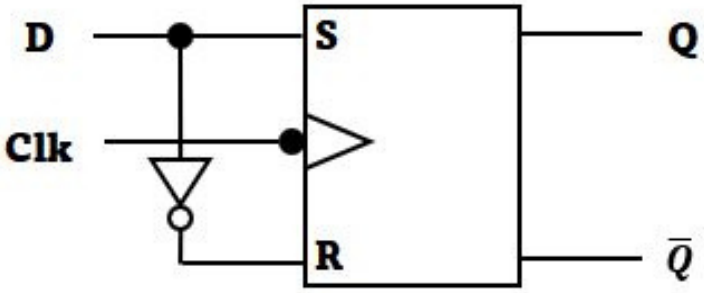
- Only have 1 input, D (Data), clock and output.
- Implementation from a JK and SR flip-flop.

Symbol

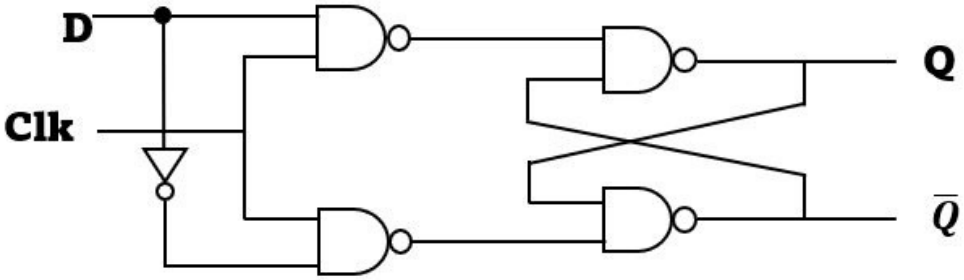


D FLIP-FLOP USING CLOCKED SR FLIP-FLOP

Block diagram



Logic Circuit

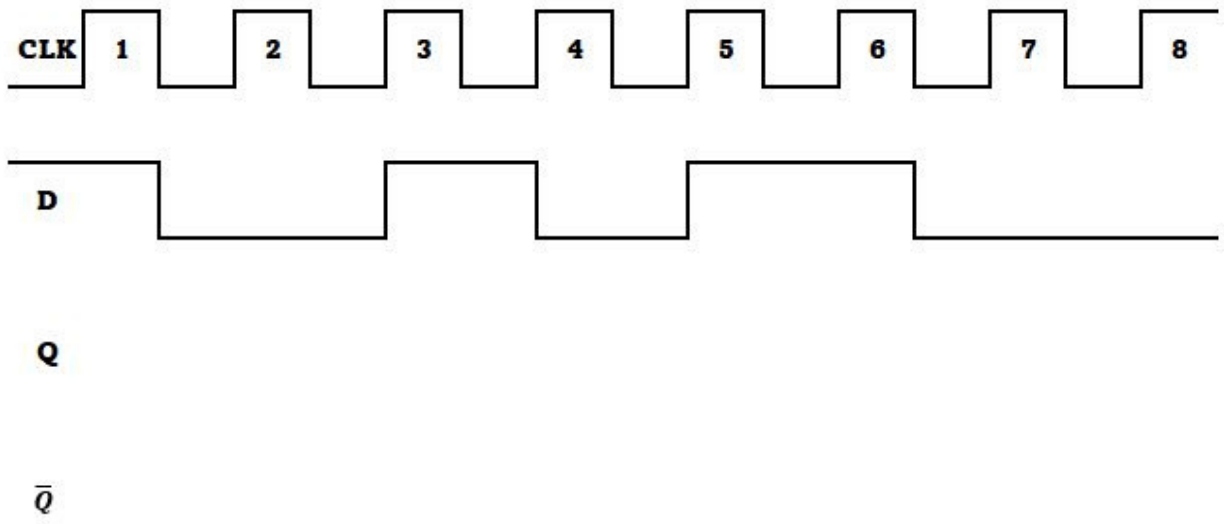


D FLIP-FLOP USING CLOCKED SR FLIP-FLOP

Truth Table

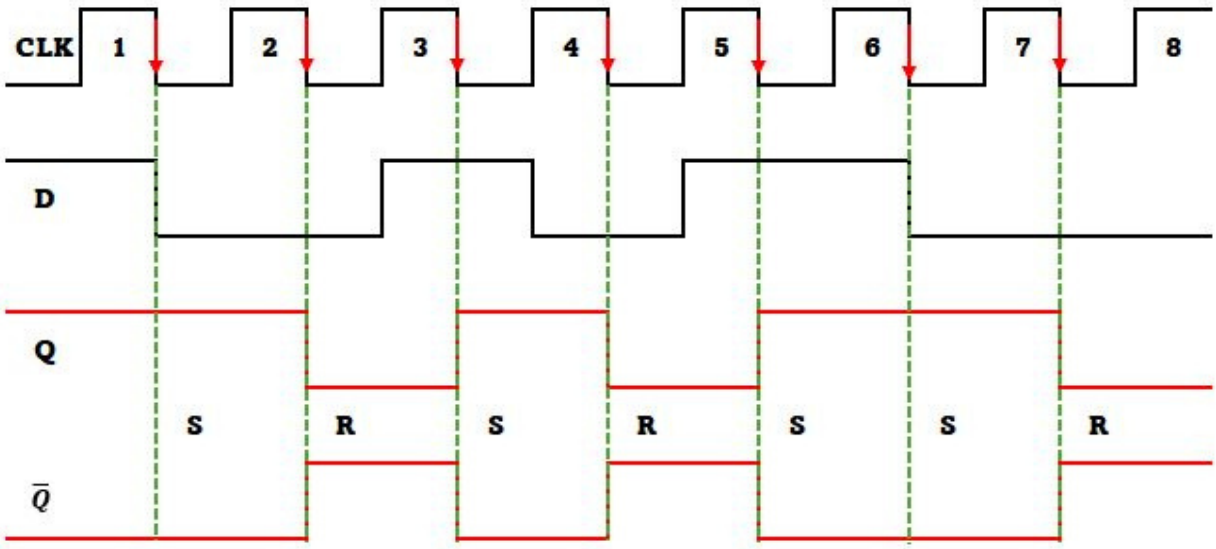
INPUT		OUTPUT		MODE OF OPERATION
CLK	D	Q	$\overline{Q}$	
1	0	0	1	RESET (R)
1	1	1	0	SET (S)
0	X	Q	$\overline{Q}$	HOLD (H)

Example 8 Draw the output Q and $\overline{Q}$ waveform for negative edge trigger D flip-flop. Initial Q is SET.



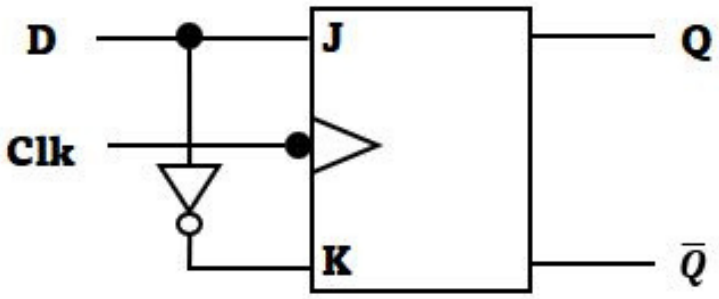
D FLIP-FLOP USING CLOCKED SR FLIP-FLOP

Example 8

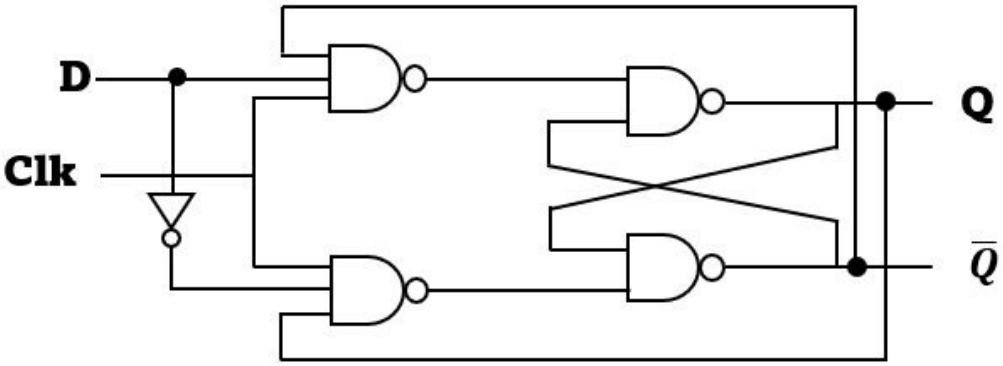


D FLIP-FLOP USING JK FLIP-FLOP

Block diagram



Logic Circuit

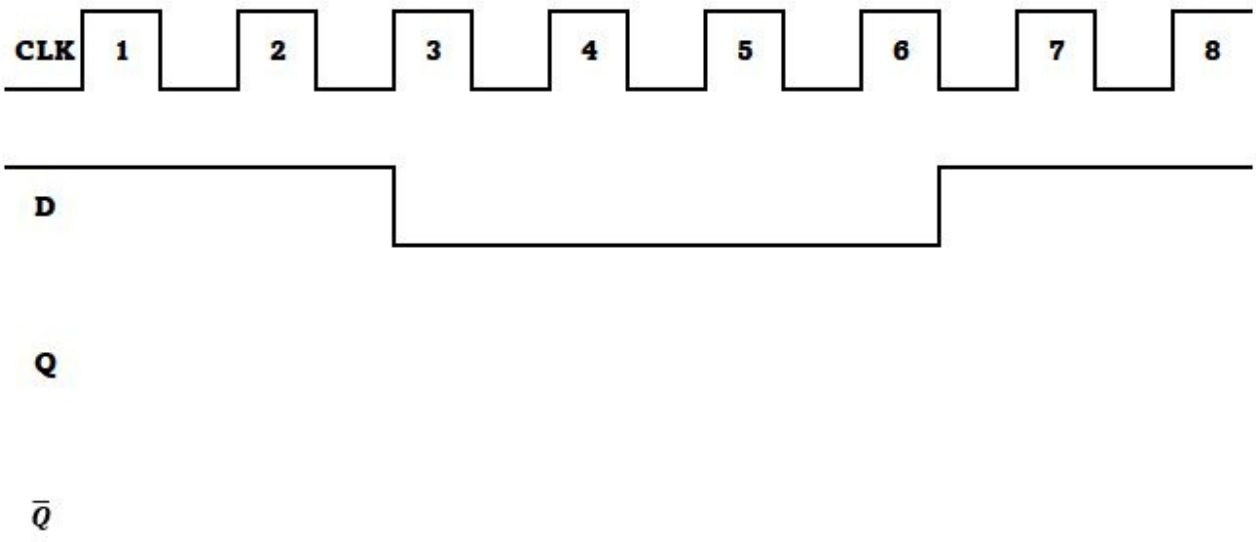


D FLIP-FLOP USING JK FLIP-FLOP

Truth Table

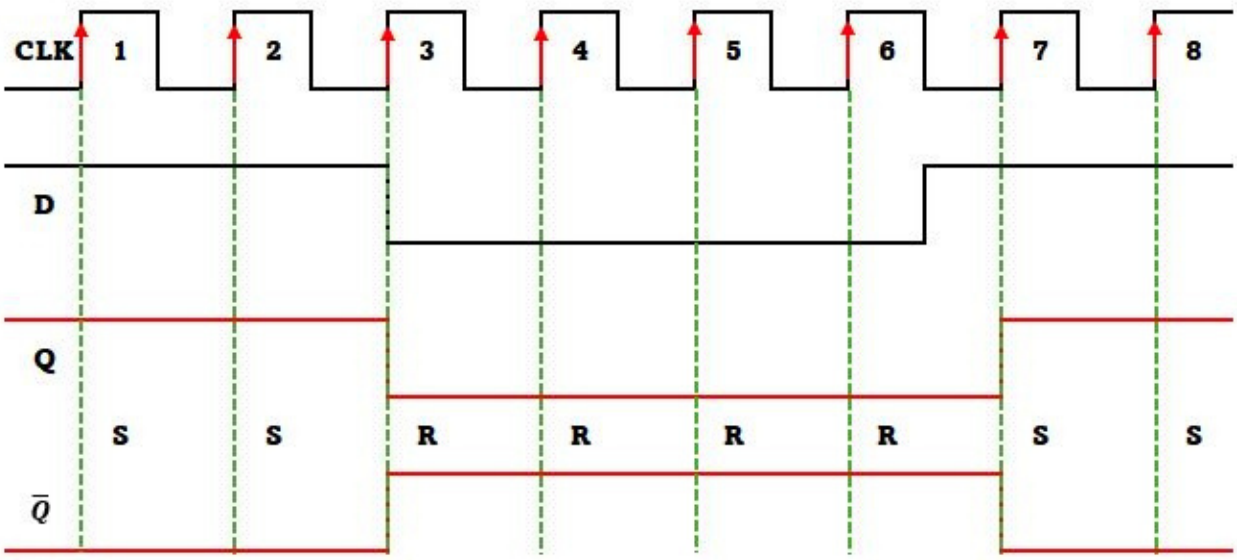
INPUT		OUTPUT		MODE OF OPERATION
CLK	D	Q	$\overline{Q}$	
1	0	0	1	RESET (R)
1	1	1	0	SET (S)
0	X	Q	$\overline{Q}$	HOLD (H)

Example 9 Draw the output Q and $\overline{Q}$ waveform for positive edge trigger D flip-flop. Initial Q is SET.



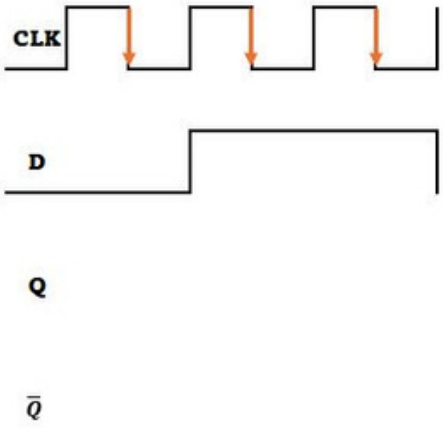
D FLIP-FLOP USING JK FLIP-FLOP

Answer 9



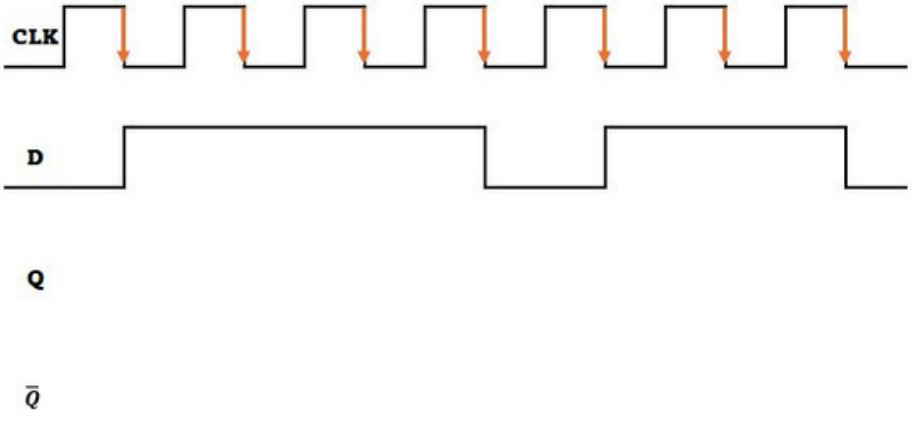
Try this!

1. Draw the output Q and $\overline{Q}$ for timing diagram in figure below. Assuming the initial Q=1.



2. With the aid of a diagram and truth table, explain how D flip-flop can be built by using SR flip-flop.

3. Draw the output Q and $\overline{Q}$ for D flip-flop in figure below. Assume Q initial is 0.



QUIZ TIME

INSTRUCTION:
Answer all question in 15 minutes

Scan me!

Submit your answer here

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